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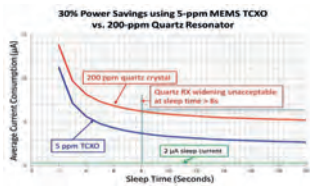
Implementing smart manufacturing



ACM is passionate about cleaning wafers



Enabling smaller, lower-power IoT & wearables



Rely on SAM for 3D package device analysis



Structural defects in TO-22



Linde

High productivity dopant source materials enable ion implant evolution

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editor's view

By Mark Andrews, Technical Editor



IC manufacturing during 2020's new normal

AS THIS ARTICLE IS WRITTEN, our industry is a week away from SEMICON West – If this were a 'business-as-usual' time I would be packing, updating my interview schedule for a week in San Francisco, and doing all those other pre-trip things that an industry veteran undertakes before taking to the road. But not in 2020.

SEMICON West 2020 is a virtual event, so meetings will be attended using video conferencing platforms; our magazine trade show booth will be built of electrons in cyberspace. More changes amongst the many that all of us have had to deal with at a time when we are still trying to achieve balance between important and sometimes conflicting objectives.

Even as we think of how our school age children will attend class this fall, or the many other things that continue to change almost daily, the SEMI trade group reported that North America-based manufacturers of semiconductor equipment posted \$2.35 billion in May billings worldwide, which is 2.9 percent higher than the final April 2020 level of \$2.28 billion, and a whopping 13.1 percent higher than May 2019 billings. It seems that no matter what happens around us, technology continues to be a societal 'glue' that enables all types of work and life scenarios that were unimaginable mere months ago.

In this pre-SEMICON West edition, Linde Electronics reports on new innovations that the company has developed to radically speed ion implantation for the manufacture of advanced ICs. ACM Research describes ways that its latest wafer cleaning system additions have combined the benefits of wet bench and single chamber cleaning systems to speed cleaning while



dramatically reducing the amount of sulfuric acid used to eliminate contaminants in advanced node wafer processing. Edwards Vacuum also provides an update on ways its smart manufacturing techniques are transforming the sub-fab to enable more uptime while cutting overall costs.

'Business Unusual' continues to challenge our industry. But we have also seen resilience and growth that demonstrate how we can productively live and work safely, even within our very changed world. Stay safe – I hope to see you (virtually) at SEMICON West.

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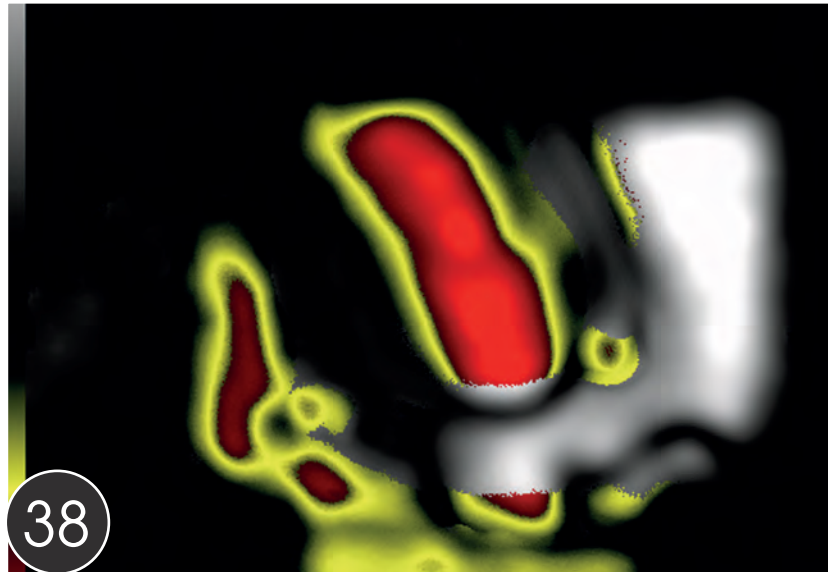
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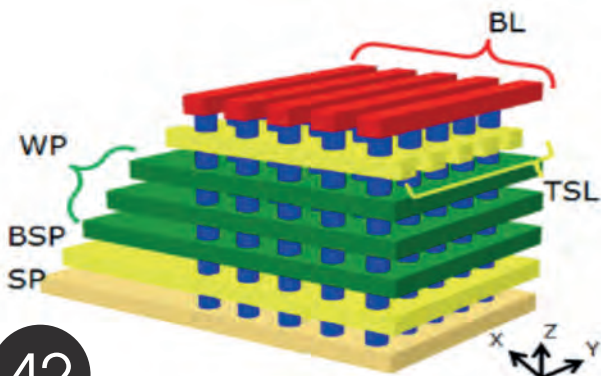
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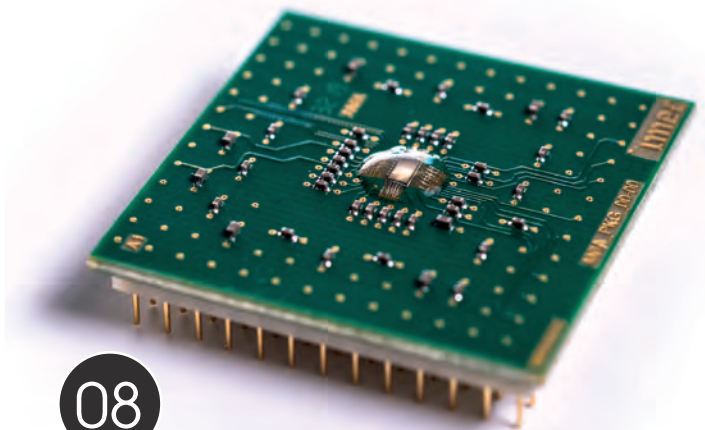
Jan Van Houdt, Scientific Director at imec, explains how the FeFET works and how this exciting 'newcomer' might fit in the next-generation memory landscape.



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130 years of Pfeiffer Vacuum

PFEIFFER VACUUM has been influencing developments in vacuum technology for 130 years. Science and industry have benefited equally from the numerous innovations developed and successfully brought to the market by this long-established company.

A key example being the turbomolecular pump, which was developed by the company in 1958 and has been integral to the market ever since. Thanks to its expertise, Pfeiffer Vacuum is still considered one of the world's market and technology leaders in this field.

When Arthur Pfeiffer founded the company in Wetzlar, Germany, in 1890, he initially devoted his attention to the production of remote ignition systems for gas lamps. Once electric light bulbs had established themselves on the market, the company founder quickly turned his attention to the new lighting technology that led him to look at the vacuum technology used in its production.

Arthur Pfeiffer quickly recognized the significance that vacuum technology could have in practically all areas of industry and research – and he subsequently concentrated entirely on

this field. Since then, Pfeiffer Vacuum has played a key role in shaping vacuum technology.

Today, customers include the Max Planck Institute, CERN, XFEL and EADS - vacuum pumps made by the Asstar-based manufacturer are even in use in the ISS space station.

There, as in many other applications, the customer's requirements are often very complex – not only with regard to the vacuum requirement itself, but also to the specifics of the system in question, the materials and products used or to be processed, and the process conditions. Automotive components, smartphones, pacemakers, textiles – vacuum technology is used for all these products and its solutions play an important role in both food production and in the pharmaceutical industry. Products and solutions from Pfeiffer Vacuum are developed for the fields of analytics, industry, research and development, coating systems and semiconductors.

Dr. Eric Taberlet, Chief Executive Officer of Pfeiffer Vacuum Technology AG: "With our durable products and customized vacuum solutions, we



are able to satisfy practically every customer requirement and to establish relationships that will endure for years to come.

At Pfeiffer Vacuum, 'sustainability' is not just an empty word. We are aware of our responsibility. And this is why, at all our locations around the world, we establish the necessary conditions to make sure that our staff enjoy working for Pfeiffer Vacuum.

We are socially committed, because we want to give something back, and we produce our products in the most energy-efficient and environmentally compatible manner possible. We have been living and breathing sustainability – by tradition – for 130 years.

Rohm announces LEDs for colour universal design

ROHM recently announced the 1608-size high accuracy blue-green chip LEDs, SMLD12E2N1W and SMLD12E3N1W. These products support the adoption of Colour Universal Design (CUD) in a variety of applications, such as fire alarm system indicator lights, industrial equipment warning lamps and public transportation information displays.

Colour is considered to be one of the most important means of communication and is used in a variety of ways – daily. However, approximately over 200 million people with P-type and D-type colour deficiencies around the world find it difficult to distinguish between red and green, possibly resulting in information being inaccurately conveyed – depending on the combination of colours used. Furthermore, since colour vision can vary from person to person,

it is difficult to perceive how different people see certain colours, which can be very inconvenient and also problematic as other people may not notice this deficiency.

As a result, there is a growing need in the society to implement Colour Universal Design that takes into account the various types of colour vision in order to deliver information accurately to as many people as possible.

Rohm succeeded in developing blue-green chip LEDs with special wavelengths. These products are ideal for implementing colour Universal Design in a wide range of devices, using a vertically integrated production system from the element fabrication stage and leveraging Rohm's strength thorough quality control.

The SMLD12E2N1W and SMLD12E3N1W are the first 1608 size LEDs to be certified by the Japanese NPO (Non-Profit Organisation), Colour Universal Design Organisation (hereafter referred to as CUDO) – making it possible to achieve colour schemes and designs that can be easily discernible by everyone, including those who cannot distinguish differences in colour.

In addition, adopting a new resin allows Rohm to significantly extend the LED lifetime while reducing the degradation of light intensity compared to conventional epoxy resins and improving the mold strength compared to the silicone resins while providing superior reliability. Rohm also offers AEC-Q102 qualified products that ensure worry-free use in automotive systems and industrial equipment demanding extreme reliability.



Canon launches FPA-8000iW semiconductor lithography system

CANON INC. announced the launch in Japan of the FPA-8000iW, the first Canon semiconductor lithography system to support manufacturing using large panels that are common in back-end processing.

Integrating a proprietary projection optical system, the FPA-8000iW i-line stepper* offers a wide exposure field and fine 1 μm † pattern resolution.

The FPA-8000iW was designed to meet the needs of manufacturers aiming for high production efficiency through the use of 515 x 510 mm organic panel substrates for Panel Level Packaging (PLP) applications.

PLP processes typically involve mounting and processing a large number of semiconductor chips on large panels in order to produce packages that can increase communication bandwidth while reducing the power consumption of high-performance computing systems, ideal for such products as CPUs and GPUs utilized by data centers.

Future PLP requirements include cost reduction and further shrinking of semiconductor packaging that protects delicate internal semiconductor circuitry from outside environments and electrically connects to external components.

The FPA-8000iW supports PLP cost reduction and package scaling by



providing high productivity panel processing with a large exposure field and high resolution. In response to packaging processes that use panel substrates, Canon developed a new stepper platform capable of handling large 515 x 510 mm panel substrates.

Severe warpage is also common in large panel substrates and the new platform and panel-feeding system can overcome up to 10 mm of panel warpage. As a result, the FPA-8000iW can help

customers realize high-productivity and efficiency for PLP production of large packages.

Canon's original projection optical system supports a wide 52 x 68 mm exposure field while achieving 1.0 μm resolution—the finest resolution† among packaging exposure systems that support panel substrate processes. These advantages enable state-of-the-art PLP technology that supports thin substrates with high-integration, enabling flexibility in electronic system design.

Presto Engineering moves to new facility

PRESTO ENGINEERING, an ASIC design and outsourced operations provider to semiconductor and Internet of Things (IoT) device manufacturers, announced today the grand opening of its new Caen Hub in France. The facility will provide IC test, qualification, and test production services primarily for communications, automotive, IoT, and industrial applications.

"Despite the recent world-wide

economic challenges, at Presto, we are experiencing a high demand for new product industrialization and ramp production in Europe," said Michel Villemain, CEO, Presto Engineering.

"This move to a modernized facility in Caen will enable us to support the growing customer demand."

The 1,850m² factory in the Caen area runs 24/7. It features a 400m² class ISO7

cleanroom and all of the necessary equipment to support the stringent qualifications of the JEDEC (Joint Electron Device Engineering Council) and AEC (Automotive Electronics Council) standards. The two-story facility houses Presto's advanced capabilities for test, qualification, and failure analysis.

The new hub is located at 5 esplanade Anton Philips, 14460 Colombelles, France.



Imec and GLOBALFOUNDRIES announce breakthrough in AI chip

IMEC, a research and innovation hub in nanoelectronics and digital technologies, and GLOBALFOUNDRIES, the specialty foundry, today announced a hardware demonstration of a new artificial intelligence chip. Based on imec's Analog in Memory Computing (AiMC) architecture utilizing GF's 22FDX solution, the new chip is optimized to perform deep neural network calculations on in-memory computing hardware in the analog domain.

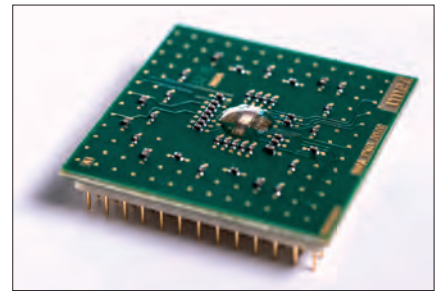
Achieving record-high energy efficiency up to 2,900 TOPS/W, the accelerator is a key enabler for inference-on-the-edge for low-power devices. The privacy, security and latency benefits of this new technology will have an impact on AI applications in a wide range of edge devices, from smart speakers to self-driving vehicles

Since the early days of the digital computer age, the processor has been separated from the memory. Operations performed using a large amount of data require a similarly large number of data elements to be retrieved from the memory storage. This limitation, known as the von Neumann bottleneck,

can overshadow the actual computing time, especially in neural networks – which depend on large vector matrix multiplications.

These computations are performed with the precision of a digital computer and require a significant amount of energy. However, neural networks can also achieve accurate results if the vector-matrix multiplications are performed with a lower precision on analog technology. To address this challenge, imec and its industrial partners in imec's industrial affiliation machine learning program, including GF, developed a new architecture which eliminates the von Neumann bottleneck by performing analog computation in SRAM cells.

The resulting Analog Inference Accelerator (AnIA), built on GF's 22FDX semiconductor platform, has exceptional energy efficiency. Characterization tests demonstrate power efficiency peaking at 2,900 tera operations per second per watt (TOPS/W). Pattern recognition in tiny sensors and low-power edge devices, which is typically powered by machine learning in data centers, can now be performed locally on this power-efficient



accelerator.

“The reference implementation not only shows that analog in-memory calculations are possible in practice, but also that they achieve an energy efficiency ten to hundred times better than digital accelerators. In imec's machine learning program, we tune existing and emerging memory devices to optimize them for analog in-memory computation. These promising results encourage us to further develop this technology, with the ambition to evolve towards 10,000 TOPS/W”.

Looking ahead, GF will include AiMC as a feature able to be implemented on the 22FDX platform for a differentiated solution in the AI market space. GF's 22FDX employs 22nm FD-SOI technology to deliver outstanding performance at extremely low power, with the ability to operate at 0.5 Volt ultralow power and at 1 pico amp per micron for ultralow standby leakage.

Analog Devices announces collaboration with Maxim

ANALOG DEVICES and Maxim Integrated Products has announced that they have entered into a definitive agreement under which ADI will acquire Maxim in an all stock transaction that values the combined enterprise at over \$68 billion. The transaction, which was unanimously approved by the Boards of Directors of both companies, will strengthen ADI as an analog semiconductor leader with increased breadth and scale across multiple attractive end markets.

Under the terms of the agreement, Maxim stockholders will receive 0.630 of a share of ADI common stock for each share of Maxim common stock they hold at the closing of the transaction. Upon closing, current ADI stockholders will own approximately 69 percent of the combined company, while Maxim stockholders will own approximately 31 percent. The transaction is intended to qualify as a tax-free reorganization for U.S. federal income tax purposes.

“Today's exciting announcement with Maxim is the next step in ADI's vision to bridge the physical and digital worlds. ADI and Maxim share a passion for solving our customers' most

complex problems, and with the increased breadth and depth of our combined technology and talent, we will be able to develop more complete, cutting-edge solutions,” said Vincent Roche, President and CEO of ADI. “Maxim is a respected signal processing and power management franchise with a proven technology portfolio and impressive history of empowering design innovation. Together, we are well-positioned to deliver the next wave of semiconductor growth, while engineering a healthier, safer and more sustainable future for all.”

“For over three decades, we have based Maxim on one simple premise – to continually innovate and develop high-performance semiconductor products that empower our customers to invent. I am excited for this next chapter as we continue to push the boundaries of what's possible, together with ADI.

Both companies have strong engineering and technology know-how and innovative cultures. Working together, we will create a stronger leader, delivering outstanding benefits to our customers, employees and shareholders,” said Tunç Doluca, President and CEO of Maxim Integrated.



Traditional PC shipments continue to grow amid global slowdown

THE SECOND quarter of 2020 (2Q20) ended well for the Traditional PC market, comprised of desktops, notebooks, and workstations, with global shipments growing 11.2% year over year reaching a total of 72.3 million units, according to preliminary results from the International Data Corporation (IDC) Worldwide Quarterly Personal Computing Device Tracker. As restrictions around the world tightened in the first few weeks of the quarter, demand for notebooks continued to grow to maintain continuity of business and schooling for many communities.

Despite logistics issues early in the quarter, the cost and frequency of both air and sea freight inched closer to normal (i.e. pre-COVID levels). This,

combined with PC production ramping up (and in some cases surpassing previous levels), meant that retailers and other distributors around the world had ample supply and were ready to fulfill the surge in demand.

“The strong demand driven by work-from-home as well as e-learning needs has surpassed previous expectations and has once again put the PC at the center of consumers’ tech portfolio,” said Jitesh Ubraniresearch manager for IDC’s Mobile Device Trackers. “What remains to be seen is if this demand and high level of usage continues during a recession and into the post-COVID world since budgets are shrinking while schools and workplaces reopen.”

CyberOptics will launch a WX3000 system for 12” and 8” wafers

CYBEROPTICS, a developer and manufacturer of high-precision 3D sensing technology solutions, will unveil the new Multi-Reflection Suppression (MRS)-enabled 3D and 2D WX3000 Metrology and Inspection systems for wafer-level and advanced packaging applications at the virtual SEMICON West show, July 20-23rd.

Incorporating the NanoResolution MRS sensor, the WX3000 Metrology and Inspection systems enable the ultimate combination of high speed, high resolution and high accuracy for wafer-level and advanced packaging, to improve yields and productivity.

Performing two to three times faster than alternate technologies at data processing speeds in excess of 75 million 3D data points per second, the NanoResolution MRS sensor-enabled WX3000 systems deliver throughput greater than 25 wafers per hour. 100% 3D and 2D metrology and inspection can be completed simultaneously at high speed, as compared to an alternate, slow method that requires two separate scans for 3D

and 2D and only a sampling of a few die. The proprietary NanoResolution MRS sensor, deemed best in class, meticulously identifies and rejects multiple reflections caused by shiny and mirror-like surfaces. Effective suppression of multiple reflections is critical for highly accurate measurements.

“With the growing complexity and variety of advanced packaging, the need for highly accurate, 100% 3D and 2D metrology and inspection continues to increase,” said Dr. Subodh Kulkarni, President and CEO, CyberOptics,

WX3000 systems are designed specifically for various wafer-level and advanced packaging applications including wafer bumps, solder balls and bumps, gold bumps and copper pillars.

The systems provide superior measurement and inspection performance for features down to 25-micron, including bump height, coplanarity, diameter and shape, relative location and a variety of other measurements.

Entegris acquires GMTI

ENTEGRIS has announced it has acquired Global Measurement Technologies Inc. (GMTI), an analytical instrument provider for critical processes in semiconductor production, and its manufacturing partner Clean Room Plastics, Inc. Located in Chandler, Arizona, GMTI is now part of the Advanced Materials Handling (AMH) Division of Entegris.

GMTI is a market leader in the design and production of high precision analytical instruments for Chemical Mechanical Planarization (CMP) slurries and formulated cleaning chemistries used in the semiconductor manufacturing process. GMTI’s technology is designed to ensure precise consistency of complex blended chemistries to enable high yields in the CMP and formulated cleaning processes.

“The acquisition of GMTI enhances Entegris’ position as the premier supplier for yield enhancement solutions for the semiconductor market. Greater materials intensity and greater materials purity will be the primary defining factors of the next generation of semiconductor performance,” said Bertrand Loy, President and CEO of Entegris. With the combination of GMTI’s cutting-edge measurement systems and our extensive portfolio of filtration and other contamination control solutions, we bring a complete suite of solutions that allow our customers to achieve process stability and high yields in the complex CMP environment. We are very excited about joining Entegris. The combined portfolio, global infrastructure and operational resources will allow us to deliver significant value to our customers.,” said Bryan LaFlam, President of Global Measurement Technologies Inc.

Entegris acquired Global Measurement Technologies Inc. for an aggregate amount of approximately \$36 million in cash, subject to customary post-closing adjustments.

High productivity dopant source materials enable ion implant evolution

Ion implantation has become a key enabling process in semiconductor fabrication. However, some of the newest implant species present challenges that can slow production. Linde Electronics has pioneered new technology to accelerate species implantation and help ensure high quality.

BY DR. ASHWINI SINHA, ASSOCIATE DIRECTOR R&D, LINDE ELECTRONICS

THE INTRODUCTION of ion implantation for IC device fabrication can arguably be regarded as a pivotal development which enabled economic viability and eventually ubiquitousness of electronics in our lives. Its ability to place desired atoms in a substrate with a very precise location, dose and depth control enabled high manufacturing yield and product reliability that were critical to achieving the desired economy of scale and unit cost reductions. Today, the ion implant process is used to implant over 15 different atomic species for a variety of applications.

Figure 1 illustrates the evolution of implant species as they entered high volume manufacturing.

Boron, phosphorus and arsenic have been long standing choices for *p* and *n* type dopant species primarily used to modify electrical properties of

the doped substrate. Continuous shrinkage of device sizes and evolution of more complex device architecture brought the need for thinner films with shallow implant depths, higher dosing, and non-electrical material modifications. This led to the introduction of several new implant species in the product mix. Most notable among the second generation of species included germanium, carbon, silicon, and fluorine. However, these new implant species and tighter process windows in turn revealed challenges with tool operation that impacted final device performance and process line productivity.

Recently, a third generation of implant species are either becoming mainstream or are candidates for next-generation process flows. Selenium is being explored to reduce contact resistance while aluminum and antimony are finding more use with the growth



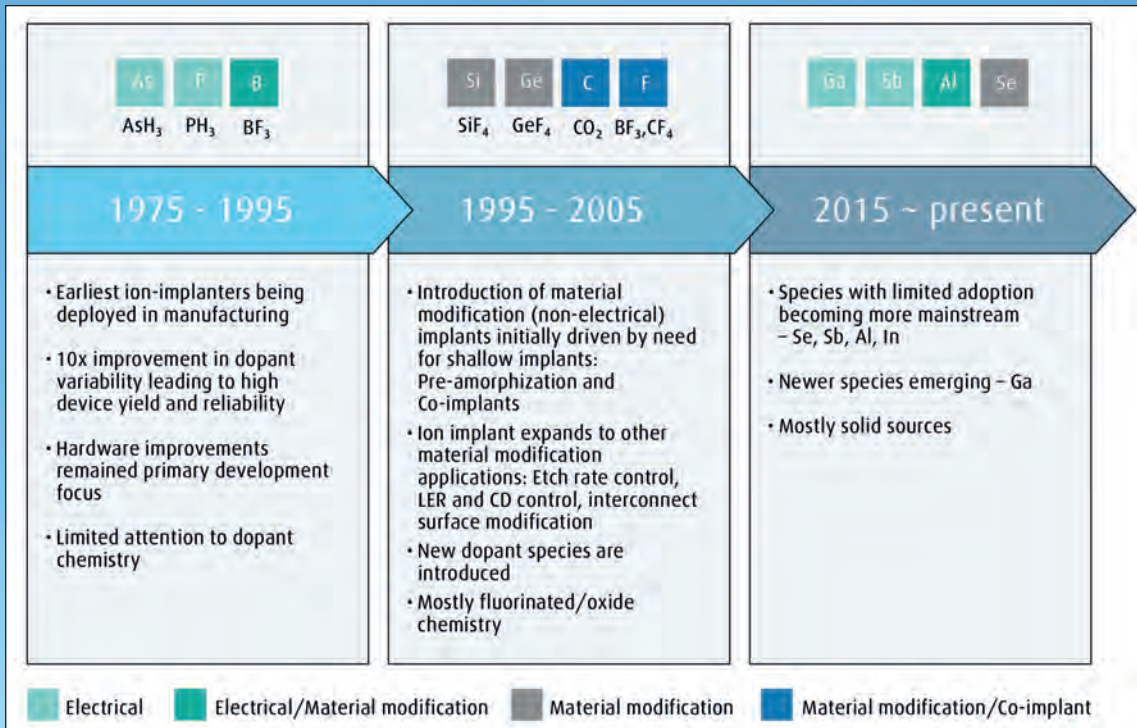


Figure 1. Evolution of implant species and source materials for beamline ion implant.

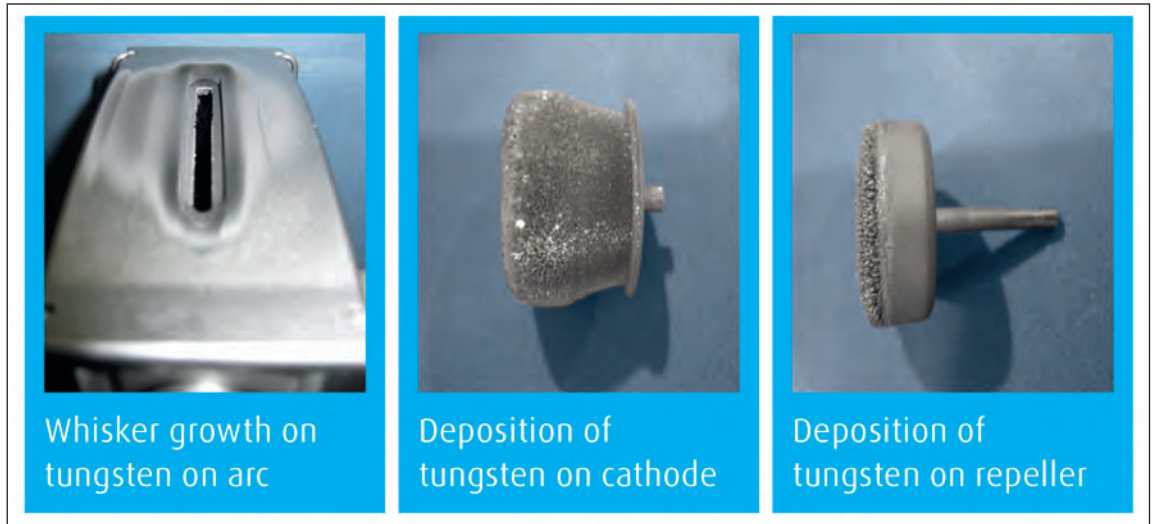
in the power devices segment. Gallium is emerging as a potential *p*-type dopant for shallower junctions. Coincidentally, the traditional sources for all these new entrants are solids, which presents a new set of issues in material handling and ion-beam optimization. In this article, we describe the productivity challenges associated with conventional sources for these new generation dopant species. Both chemistry and physics inside the tool must be addressed to resolve these challenges and deliver commercially viable implant processes. We illustrate this approach through two case studies describing high productivity performance enabled via new dopant source materials.

Fluorinated species and solid sources – a tool productivity killer

Fluorinated gases are preferred for implant dopant sources due to their favorable ionization behaviors and volatilities. Hence it was natural to adopt a fluorinated version of the dopant element to serve as the dopant source. However, the fluorinated products generated in the arc chamber plasma strongly react with the components of an arc chamber that is primarily made of tungsten or molybdenum. The interplay of fluorinated chemistry with the arc chamber leads to whisker-like growth of tungsten on arc



Figure 2. Examples of adverse effects of halogen cycle on the arc chamber components of the ion implant tool



chamber components such as the cathode, repeller and aperture [Figure 2], and on other components of the ion source such as the extraction electrodes and isolation components. This phenomenon is also known as Halogen-Cycle. Oxide species present very similar sets of issues due to the formation of tungsten oxide in the arc chamber. Eventually this leads to the failure of the ion source; tool operation is halted, and the ion-source has to be rebuilt before resuming operation. This phenomenon is the cause of the most common failure modes experienced during operation of implant tools, which we list below.

1. **Beam glitches:** Deposition on cathode, repeller and electrodes
2. **Defects:** Undesirable W growth in ion-source / beamline, compounded by beam glitches
3. **Beam non-uniformity:** Deposition on aperture
4. **Electrical shorts:** Deposition in isolation bushing

Previously, applications were equally weighted towards fluorides (BF_3) and hydrides (AsH_3 and PH_3) as the dopant source materials. Implant engineers were able to alternate between hydride and fluorinated species, and the hydrides acted as cleaning agents to reverse the adverse effects of fluorinated species. However, now the application mix is heavily weighted

towards fluoride and oxide processes, and this solution is no longer possible. The introduction of these second-generation implant source materials emerged as a tool productivity killer with a halogen cycle as the leading cause. The engineers were finding it difficult to deploy these new applications without addressing this serious issue.

Increasing demand for the new entrants like antimony, aluminum, selenium and gallium (etc.) in the product mix is adding a severe burden on tool productivity. Coincidentally, currently available options for all these implant species are solids at ambient conditions. Reliably transporting dopant material to the arc chamber thus becomes a key factor affecting implant productivity.

A typical gas base source material is packaged in a cylinder and connected to the ionization chamber using a tubing manifold - a convention for process tools in IC fabrication. When the dopant gas is demanded to start the implant process, the gas-based dopant material can be readily transported to the arc chamber precisely controlled using a mass flow controller (MFC).

Metric	Gas Sources	Solid Sources	Productivity Implications
Material delivery mode	Standard cylinders	Thermal or chemical evaporation	Additional hardware required Added PM steps 5X - 15X longer beam transitions
Flow control	MFC based - Precise	Limited	Poor dose control
Tool flexibility	High	Poor	Likely dedicated operation

Figure 3: Productivity challenges with solid sources

Implant species	Traditional implant sources	Optimized source mixtures and molecules
Alternatives for fluoride and oxide sources		
B, BF ₂	BF ₃	BF ₃ /B ₂ H ₆ /H ₂
Ge	GeF ₄	GeF ₄ /Xe/H ₂
Si	SiF ₄	SiF ₄ /Si ₂ H ₆
C	CO ₂	CO, CO/Xe/H ₂ , CO/CF ₄
Alternatives for traditional solid sources		
Sb	Sb ₂ O ₃ (s), SbF ₃ (s)	SbF ₅ (l)
Se	SeO ₂ (s), H ₂ Se	SeF ₆ (g)

Both natural and isotopically enriched analogs applicable
 (s) = solid, (l) = liquid, (g) = gas

Figure 4. New UpTime® products improving fab productivity

Unfortunately, solid sources need new hardware to enable delivery of the dopant material to the arc chamber. This includes a complex integration of hardware like thermal vaporizers or chemical volatilization of a solid target placed inside the arc chamber. Low productivity implications associated with such approaches are listed in figure 3.

Switching to an implant recipe using a gas dopant source involves a simple step of initiating its desired flow fed into the arc chamber. On the other hand, switching to a solid implant source must undergo several additional sequence steps. First, the material needs to be heated to the desired temperature and a stable vaporization rate must be achieved. Beam tuning needs an additional feedback sequence with the vaporizer because vaporization rates vary as a function of the mass of the solid source in the vaporizer.

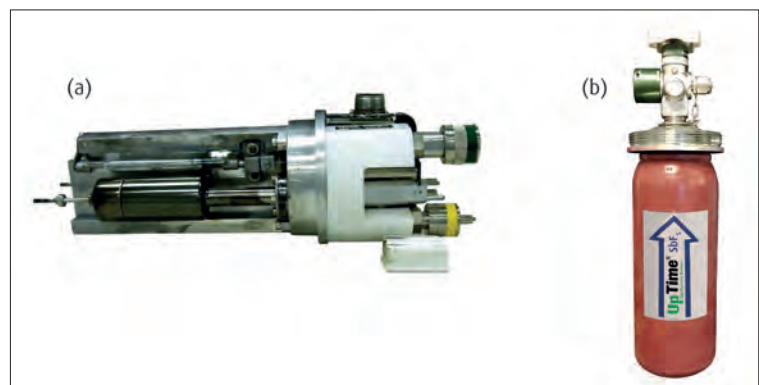
These sequences can take between 40 to 80 minutes, which is usually achieved in less than 10 minutes for a typical gas source. The implant tool needs to switch between different implant recipes involving different dopants. Evidently, a long transition time between a solid dopant source and another dopant source is highly undesirable. Additionally, once vaporized, the vapors tend to redeposit as solid form in cold spots, which necessitates long preventive maintenance procedures at regular intervals. On average, a solid-source based implant process exhibits 20%-30% lower productivity compared to a gas-source based process. Low implant productivity associated with

solid sources has been the primary reason for their low adoption. The tool productivity bottleneck must be addressed for these new species to be a viable process to enable economical process scale-up of these emerging devices.

Developing implant chemistry

During the first generation of tools and processes, ion implant development was driven primarily by physics: ionization, ion selection, and strength, energy, and shape of the ion beam. With the second generation of processes and source materials, the heavy load of fluorinated chemistry in the recipe mix became an issue, as demonstrated above by the problems with the halogen cycle. In this section, we describe our approach to develop optimized source materials which addresses both the physics and chemistry requirements of newer ion implant processes to enable high tool productivity and device performance.

Figure 5. Advancing from (a) solid vaporizer to (b) preferred gas cylinders



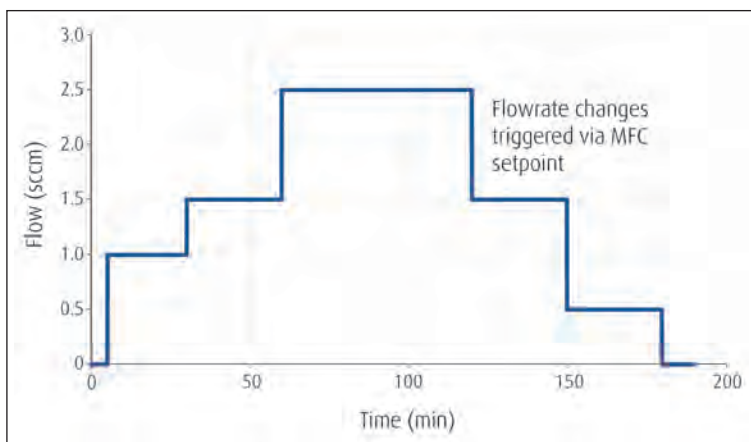


Figure 6: SbF_5 flow via MFC control

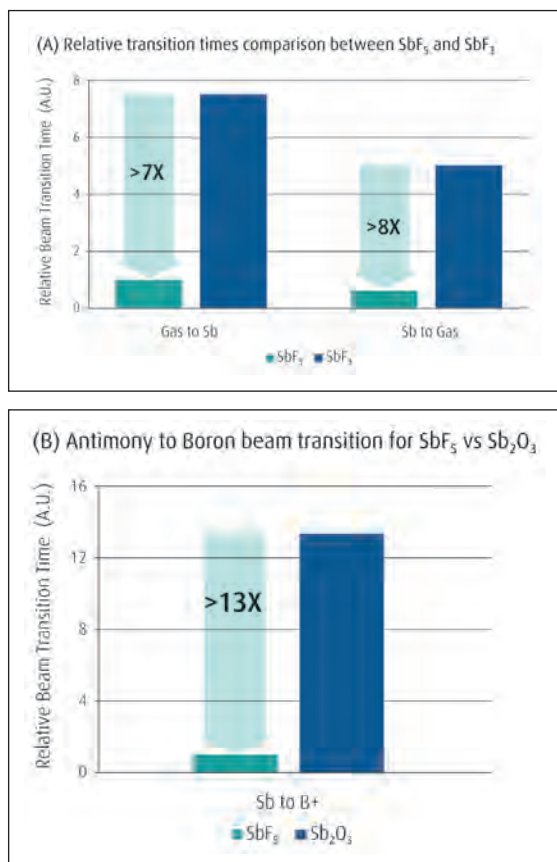


Figure 7: Faster beam transitions and startup time with SbF_5 .

We will also present our efforts to develop alternate gas-like dopant sources to offset the shortcoming displayed by conventional solid dopant sources.

It is important to note that because deposits continue to build up during the halogen cycle, it is not effective to implement a post-implant clean solution to remove the previously formed deposits. Not only does such a cleaning option result in unacceptable variability between cleaning cycles, but they also incur additional equipment downtime while post implant cleaning is being performed. The more effective approach is to implement in situ measures to abate the active fluorine ions/neutrals generated during initiation and disrupt the halogen cycle. This can be achieved by co-mixing

a suitable chemistry with the fluorinated implant source materials.

While addressing the chemical problem, one must also retain the physics performance of the tool, as indicated by the key metric of beam current. Hence, the overall challenge is to solve and optimize both sets of variables: identifying a gas chemistry which extends tool uptime and reduces variability while maintaining high beam current. Appreciating the challenge, Linde designed and built an ion-implant test stand to develop novel gas chemistry solutions to enable high productivity for the implant process. With the deep understanding of both implant process physics and gas-phase chemistry, we invented novel dopant source solutions that not only mitigate the halogen cycle or oxygen attack but also increase the beam currents to further improve the implant tool throughput. The test system is designed to rapidly screen and optimize different gas chemistries, and thus significantly reduce the cycle time for implant process owners to deploy the best-in-class solutions. Figure 4 lists several new dopant sources currently offered by Linde that are driving implant tool productivity by delivering high marks on all the key metric listed in the section above. The two case studies presented below showcase the benefits implant process owners derive by implementing these novel solutions.

Case study 1 – Gas-like dopant source for antimony implant

Antimony (Sb) is another candidate for n-type doping besides arsenic and phosphorus. Antimony in fact has superior transports characteristics due to low diffusion coefficient and is a choice dopant candidate for Si based power devices. However, its adoption has been limited due to unavailability of a gas-based source. Traditionally, only solid sources like SbF_3 , Sb_2O_3 or metallic Sb have been used as a dopant source. Solid sources are usually delivered via a vaporizer assembly where solid dopant sources are placed in a crucible very close to the arc chamber. The crucible is heated to an elevated temperature ($250^\circ\text{C} - 1,000^\circ\text{C}$) to volatilize the solids kept in the crucible and then transported via a carrier gas flowing over the hot crucible.

This delivery approach suffers from several limitations which are nearly absent for a gas-based source.

- Long recipe / beam transition times: Long heat-up/cool down of vaporizers for every transition. Typical transition times are in the range of 60-80 mins
- Limited crucible lifetime: ~60-100 hrs
- Limited flow control: Poor dose control
- Redeposition of solids on colder surfaces: Defects and frequent preventive maintenance requirements

Beam transitions from Sb to B is particularly so difficult that it can take up to 60 mins just to stabilize to a desired beam specification. This phenomenon is often referred to as “Antimony-Sickness.” Currently implant engineers’ only option to avoid these long beam transitions is to dedicate the implant tool solely

for antimony implant – a significant reduction of manufacturing flexibility and tool productivity.

Taken together, these limitations have prevented a wider adoption of Sb doping processes despite superior device properties like a shallower implant profile and reduced auto-migration in comparison to As. Linde recently introduced a gas-based source for Sb in the form of antimony pentafluoride (SbF_5) packaged in a Linde proprietary cylinder [Figure 5]. This new Sb-source not only replaces the very cumbersome vaporizer operation but also offers several favorable properties:

- 7-10 torr vapor pressure at ambient conditions: can be easily dispensed as a gas via standard ion-implant gas stick
- Flow control via mass-flow controllers: instant flow change response
- Favorable ionization behavior: high Sb^+ and Sb^{++} generation
- Compatibility: operates with standard gas manifold components

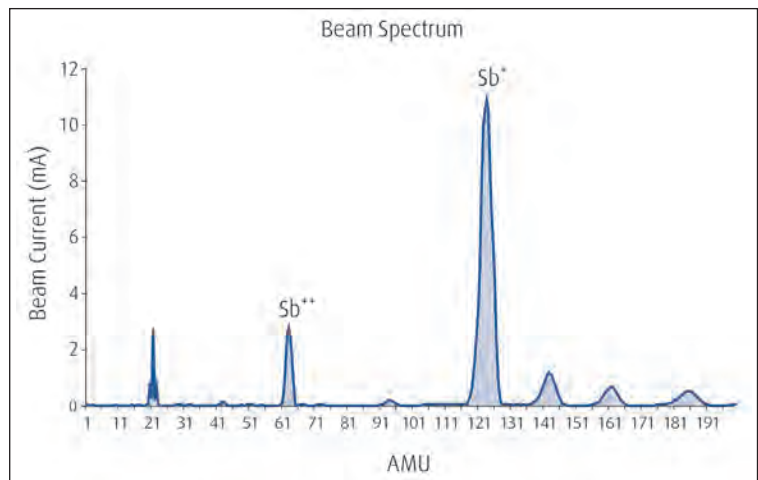
Figure 6 shows delivery of SbF_5 at different flows controlled via MFC. SbF_5 is delivered via a standard cylinder stored under ambient condition. A desired flow of Sb containing SbF_5 can be established instantly when the implant engineer needs to start a Sb beam. Similarly, the flow of Sb can be instantly shut-off by isolating the MFC and setting the target value to zero when the recipe needs to transition from Sb to any other species. The ability to deliver Sb dopant species to the arc chamber instantly in a reliable and controlled manner offers the engineers a powerful lever for improving the implant tool productivity. Implant users can use SbF_5 just like any other gas source and eliminate the productivity loss associated with incumbent solid source-based Sb implant process.

Figure 7 illustrates the relative improvement in beam transition time achieved using SbF_5 as the dopant source for Sb implant.

As noted before, retaining the physics performance of the beam current is equally important to the chemistry improvements. Figure 8 displays the excellent ionization behavior of SbF_5 resulting in high Sb^+ and Sb^{++} ion intensity. Finally, SbF_5 has also been demonstrated to deliver long source lifetime of over 300 hours across different implant tool platforms. H_2 , or a mixture of H_2 with rare gases like Ar, Kr or Xe, dispensed along with the SbF_5 vapor, serves as a robust mitigant for the halogen cycle and enable the desired source lifetime [Figure 9]. Full product qualification is currently underway at several device manufacturers.

Case Study 2 – Novel dopant source mixture for high dose low energy boron implant

Boron is the most widely implanted specie in an IC device and is usually doped in the form of B^+ and BF_2^+ ions. However, the dosing and implant energy



required varies widely among the application device types and specific process applications.

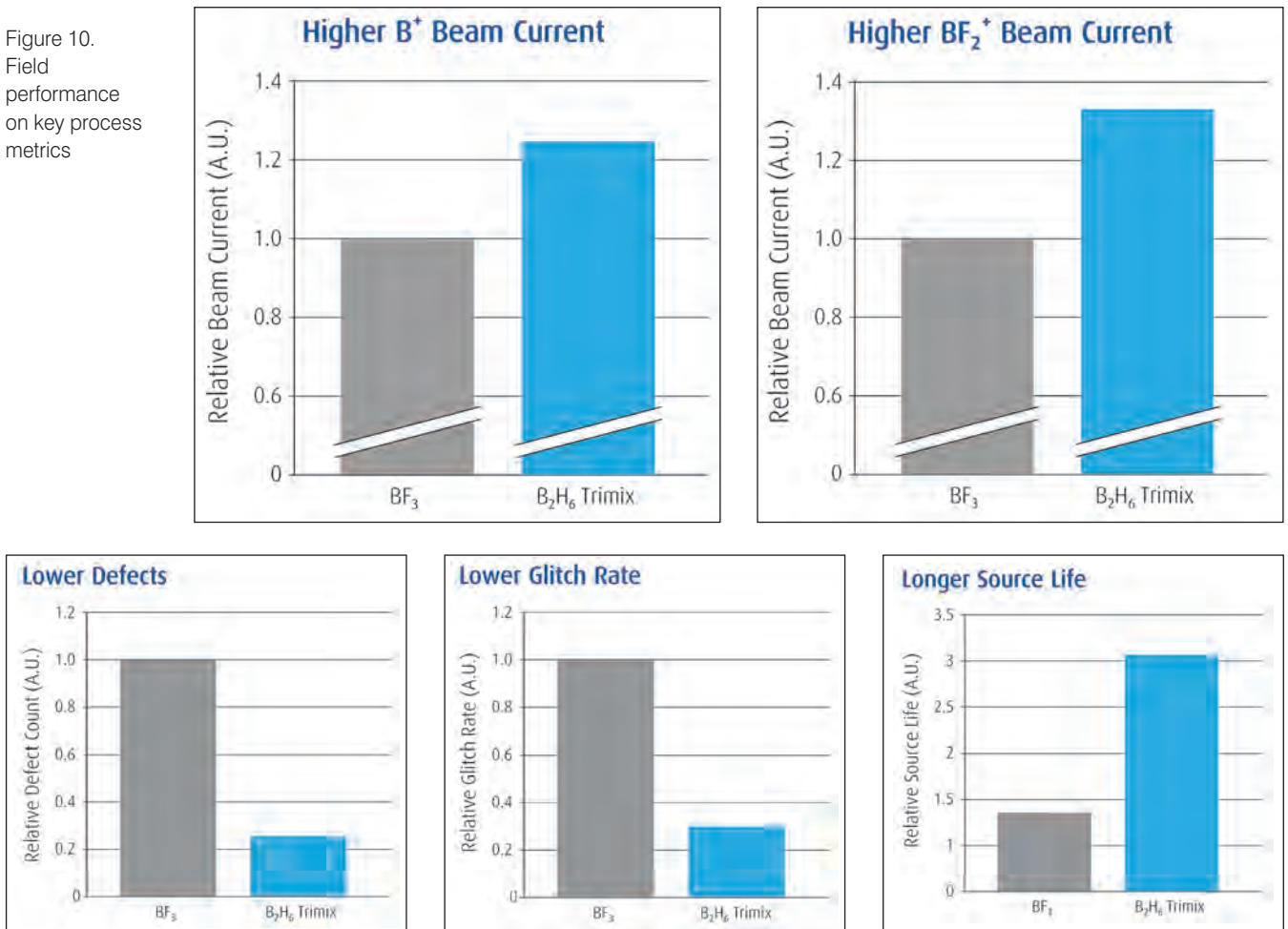
Figure 8. SbF_5 ionization performance

Continuously shrinking device dimensions and the advent of FinFET architectures pushed certain boron recipes into the very high dose (E15 – E16 atom/cm² and low energy (sub 1 keV) implant regime. These high-dose, low-energy implants are much more challenging than other boron recipes. First, the implant tools are usually beam current limited at these low energies, significantly reducing the



Figure 9. Clean operation: 300+ hours dedicated operation.

Figure 10. Field performance on key process metrics



wafer throughput. While the average throughput for other recipes are in the range of 50 -100 wph, the throughput for these recipes can be limited to 15-30 wph. Secondly, these low energy implant layers are usually very sensitive to beam glitches and defects. It is not uncommon that the ion-source failure may happen due to the inability of the implant tool to achieve beam spec requirements for one of these high-dose, low-energy recipes. There was a clear need to develop solutions to improve beam current (equipment throughput) and ion-source lifetimes for tools running these recipes.

Linde has developed a patented mixture of B_2H_6 , H_2 and BF_3 (Boron Trimix) which is being widely adopted by IDMs to improve the productivity of their boron implant. Linde also utilized the advantage of its UpTime[®] based sub-atmospheric delivery system to package the mixture in a single container and avoid the need for a separate gas manifold to deliver this mixture to the ion-source chamber. Detailed mechanism behind improved performance with this novel gas mixture is described in US Patent 9,570,271.

Figure 10 shows the summary of benefits that customers have been able to realize by use of Boron Trimix in their fabs. These benefits continue to enable implant engineers to meet stringent process

requirements for these evolving high-dose, low-energy boron implants and to deliver on fab productivity targets.

Conclusion

As technology roadmaps evolve and more varied and complex thin films are required, ion implantation will undoubtedly be employed extensively to introduce new dopant species to meet developing device requirements. To support these new applications, innovation creating new material sources will also be required. As illustrated in the above case studies, both physics and chemistry of the dopant sources must be co-optimized to achieve a viable commercial offering and process scale-up.

Linde has pioneered development of novel dopant sources that has enabled implant process users to increase their equipment throughput, reduce equipment failures and improve process yields. By using Linde's proprietary screening test stand and protocols, we have rapidly prototyped new materials to support our customers' process screening, validation, and optimization. These novel dopant materials, in combination with UpTime innovative packaging, offer the best suite of products and lowest cost-of-ownership solutions for ion-implant processes.

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Panasonic

ACM Research is passionate about cleaning wafers

The critical importance of wafer cleaning grows with each new semiconductor node. As geometries shrink, even minute contaminants have outsized impacts. Particles that didn't effect performance at the 28nm node can become 'killers' at 10nm and below. ACM Research elevates wafer cleaning to new heights by not only reducing contaminants but also slashing waste, setting sights on building 'win-win' customer relationships in a highly competitive corner of the global IC process tool industry.

BY: MARK ANDREWS, TECHNICAL EDITOR



David Wang,
CEO, ACM
Research

ACM Research knows a lot about cleaning wafers. The company also recognizes that wafer cleaning has become so essential to advanced nodes that effective, fast cleaning gives customers a competitive edge they need to address the complex challenge of fabricating next-generation ICs.

Through their growing portfolio of wafer cleaning and related silicon wafer production products, ACM Research has set its sights on becoming a force within what it sees as a \$5 billion (USD) TAM within the semiconductor supply chain. If you don't know ACM Research yet, chances are you'll meet them soon.

The most recent quarterly report by ACM Research included impressive numbers even as the world continues to struggle with SARS CoV-2 and the COVID-19 infection that has killed and sickened hundreds of thousands of people across the globe. The company announced first quarter revenue of \$24.3 million, a 19% increase



Right: ACM
Research
Ultra C Wet
Bench

year-on-year, with \$12 million coming from equipment deliveries. While the \$12 million in new installations was \$2 million off its 2019 record, the fact that ACM moved forward while the COVID-19 pandemic began its rampage is telling about the company's continuing ability to excite new customers under the most challenging of circumstances.

ACM Research isn't exactly an 'overnight' success story – The company got its start in Fremont, California in 1998, where it is headquartered. ACM Research added a facility in Shanghai in 2006. By 2009, ACM was supporting memory giant SK Hynix after successfully demonstrating the effectiveness and yield improvements possible with its space alternated phase shift (SAPS) system and megasonic cleaning capabilities for both flat and patterned wafers.

The company's bubble oscillation system dubbed 'TEBO' followed, proving successful in effectively cleaning patterned wafers at advanced process nodes. Orders from SK Hynix continued to grow, and in 2015 the company achieved success with cleaning 3D structures; its customer base continued to grow in Korea, Taiwan and China. Following these successes, the company went public on the NASDAQ exchange in 2017, and added a second R&D and factory facility in Shanghai in 2018. Work continued on a new system that would be dubbed Ultra C Tahoe; ACM targeted deliveries to lead customers beginning in 2019.

As device geometries continue to shrink, heading towards 5nm and below, the complexity and sheer volume of process steps is also accelerating. Wafer cleaning, either using a dry process

or one of several wet processes, is generally believed to be repeated as many as 200 times for highly advanced structures.

Because IC and microcircuit recipes vary so widely across industry, there's no precise way to calculate exactly how many more cleaning steps are added at each new node, but

one fact was immediately clear to fab operators: what worked at 28nm wasn't going to cut-it at 10nm and below. Older cleaning methodologies such as wet bench systems in which wafers are essentially immersed in a bath of reused solvent and acid chemistries with water rinses were not up to the task of removing enough contaminants to ensure that today's 7-5nm devices could deliver acceptable lifetimes at profitable yields. As new cleaning technologies were being

developed across the supply chain to meet the needs of advanced node devices, ACM Research was developing a unique approach in its Ultra C Tahoe system. From the viewpoint of company CEO, David Wang, some of the more advanced cleaning systems on the market were getting the job done, but at the expense of a sizeable uptick in the amount of sulfuric acid (H_2SO_4) they consumed, creating waste treatment and disposal problems along the way. The company believed that some cleaning systems were wedded to technologies that either used too many 'consumables' or did a relatively poor job of removing defect-causing contaminants, or both.

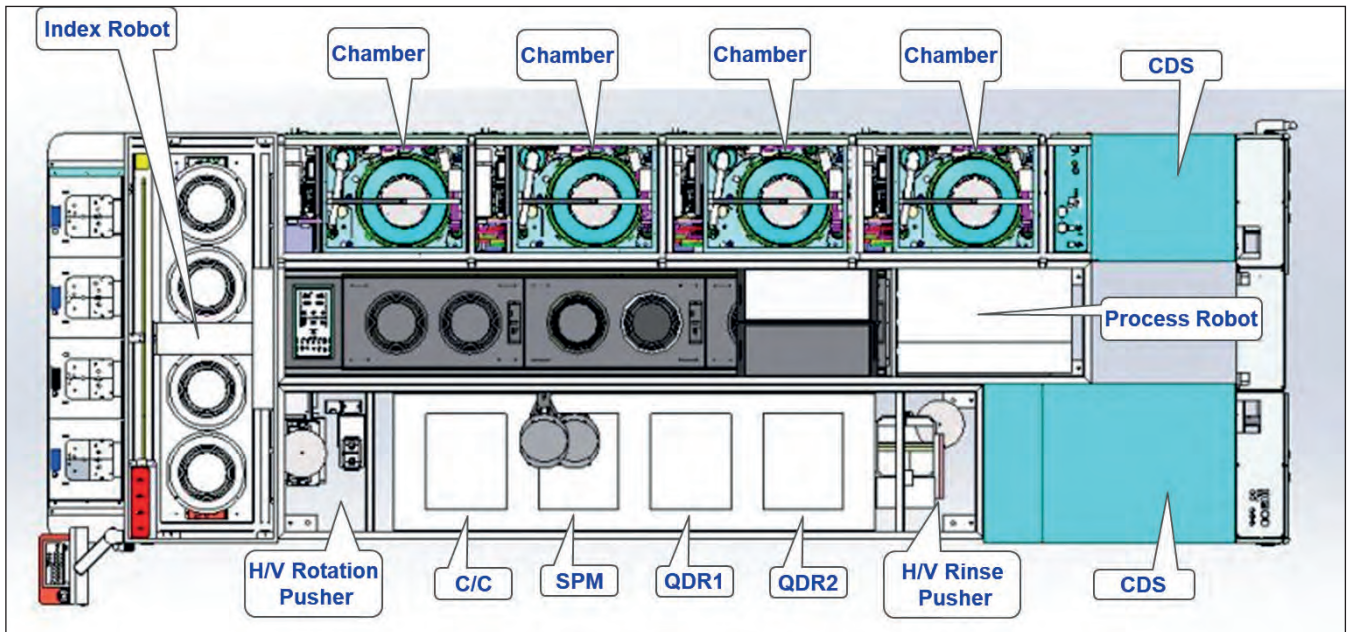
"In a typical wet bench system, a batch of wafers is dunked in the bath statically, so that it cannot achieve the cleaning efficiency of a single wafer process, where the wafer is spinning with a very thin boundary chemical diffusion layer being applied to the wafer surface," Wang remarked.

"What's more, a standalone bench process cannot eliminate the problem of cleaning inefficiency from non-uniformity across the wafer. The wafer edge cleaning efficiency cannot be as good as the wafer center, due to the geometrical limitation of the tank, the wafer guides, etc. The wafer-to-wafer, batch-to-batch cleaning performance also cannot be controlled well. However, in a single wafer process, the cleaning method is more advanced because it spins each wafer while process chemicals are dispensed onto the wafer. Additionally, supplementary cleaning methods can be added to a single wafer process, such as N_2 spray DIW and megasonic cleaning," he said.

In December 2019 ACM Research formally announced the release of its Ultra C Tahoe cleaning system. It is designed to dramatically reduce the consumption of sulfuric acid and other industrial chemicals in HVM. The company said its new Ultra C Tahoe system is the world's first tool combining bench and single wafer cleaning through an integrated approach. The new tool supports photoresist stripping and post-etch, post-implant and post-CMP cleans. The system delivers improved process performance, chemical cost savings and significantly reduced sulfuric acid waste generation that is accomplished by slashing acid consumption to approximately one-tenth that of legacy cleaning systems. Recent tests have confirmed that on average, using the Ultra C Tahoe can reduce sulfuric acid waste by 80 percent.

Wang said that his company has worked towards developing a complete system like the Ultra C Tahoe to offer customers a cost reduction strategy that addressed chemical waste issues as well as performance objectives. Waste disposal without harming the environment was a significant driving factor. The company noted that (global) government restrictions on semiconductor industry waste and awareness of environmental risks are driving increased demand for cleaning systems that can





ACM Research
Ultra C Tahoe
(inside view from
top)

reduce consumption of process chemicals without sacrificing performance. While handling, storing and dispensing hazardous acids present their own challenges, disposal methods for sulfuric acid are suboptimal.

Even though landfilling decontaminated waste remains an option in countries like the United States, it does not completely remove the risk of environmental contamination. In areas such as Korea, Taiwan and Shanghai that have limited or no landfill space available, the next waste disposal option is high-temperature purification, but this approach consumes a large amount of energy and contributes to additional greenhouse gas emissions.

The Ultra C Tahoe cleaning system combines two modules into a single wet-clean system. Sulfuric acid-peroxide mixture (SPM) cleaning and quick dump rinsing (QDR) occur in the bench module, where the SPM process chemicals are recirculated as in a stand-alone bench system, which decreases sulfuric acid waste by at least 80% compared with single wafer SPM cleaning. After bench cleaning in the Tahoe, wafers are transferred to the single wafer module for advanced cleaning while still wet.

“Sulfuric acid waste treatment is a major challenge in advanced IC manufacturing. For example, semiconductor plants account for more than half of the total sulfuric acid used in Taiwan,” said Wang. He noted that bench cleaning alone cannot achieve the required performance for 28nm nodes and below. Even as the industry has shifted to single wafer cleaning at advanced nodes to achieve improved performance, the shift dramatically increased sulfuric acid consumption and resulting waste disposal concerns. “We developed the proprietary Tahoe system to deliver the high cleaning performance and

process flexibility that customers expect from single wafer cleaning, but with a fraction of the chemical consumption. We consider this a winning combination that will enable the industry to maintain its technology roadmap with an environmentally friendly solution that saves significant money on disposal costs,” Wang explained.

The Ultra C Tahoe’s single wafer chamber is flexible and can be configured for customer-specific needs such as dispensing standard clean (SC1), hydrofluoric acid (HF), ozonated deionized water (DI-O3), or other process chemicals. It can accommodate up to four arms with up to three process chemicals on each. Options include an N₂ spray arm or megasonic cleaning with ACM Research’s Smart Megasonix arm. The system also offers an isopropyl alcohol (IPA) drying function for patterned wafers.

The Ultra C Tahoe cleaning system has demonstrated low cross-contamination risk and excellent particle-removal performance rivaling state-of-the-art single wafer systems, all at a much lower consumption rate of SPM. When compared with a traditional SPM bench tool, data from an ACM Research customer’s commercial production line demonstrated that the integrated Tahoe system can reduce particle counts from hundreds to around 10 per wafer at 30nm. A Tahoe system processing 2,000 wafers per day will consume less than 200 liters of sulfuric acid, eliminating more than 1,600 liters of sulfuric acid waste per day compared with single wafer high-temperature SPM cleaning systems.

Cross-contamination is another real issue for wafer cleaning as device geometries continue to shrink, Wang noted. In stand-alone bench systems, batches of wafers are processed in one tank, so particles, impurities or contaminants that are removed from

wafer surfaces stay in the tank and can redeposit on the wafers again. However, in a single wafer process system, the particles, impurities or contaminants that are removed from wafer surfaces are spun off by centrifugal force. Meanwhile, different process chemicals are dispensed onto the wafer surface and then spun off as well. In this way, the cross-contamination risk can be made minimal. “Because the Ultra C Tahoe combines bench and single wafer cleaning in an integrated, or hybrid system, we provide the best attributes of both,” Wang remarked.

When ACM announced availability of Ultra C Tahoe, the system was already being evaluated by a lead customer. During first quarter 2020, that customer completed its evaluation, issuing ‘first tool acceptance,’ which bolstered quarterly revenue. Performance met or exceeded expectations; Wang announced during the company’s earnings call that a second Ultra C Tahoe system had been ordered by their first Tahoe customer, and that a new North American sales vice president had been added; the company’s staffing also increased in other major semiconductor markets.

In early May, the company announced that it was expanding its line of ‘Ultra C’ cleaning systems, with new tools targeting different and complementary portions of the wafer cleaning market. The three new Ultra C tools target advanced IC, power device, and advanced WLP markets for front and backside cleaning requirements.

ACM described its Ultra C b (backside) tool as a cost-effective cleaning system that provides good particle performance and etch uniformity control for three key applications: backside metal removal or RCA clean; backside silicon etching for wet wafer thinning, or wet through-silicon via (TSV) reveal— additionally, it supports backside film removal on poly silicon, oxide and nitride layers for wafer recycling. With features that help mitigate high warpage, the system is especially well suited for processing 200mm or 300mm ultra-thin wafers and bonding wafers. The company said its new Ultra C wb (auto bench) tool performs batch cleaning of up to 50 wafers, utilizing the same advanced wet bench technology developed for ACM’s Ultra C Tahoe tool. Key applications for the auto bench include pre-furnace clean, RCA clean, photoresist strip, oxide etch, silicon nitride removal, and removal of FEOL poly/oxide or BEOL metal for wafer recycling.

The tool is configured with different tanks of chemicals, such as sulfuric acid, phosphoric acid, hydrofluoric acid (HF), buffer oxide etchant (BOE), SC1 and SC2 for a specific application step. Wafers are successively dipped in the baths, rinsed with deionized (DI) water, and dried with an ATOMO dryer using vaporized isopropyl alcohol (IPA), leaving no watermark. ACM described its new Ultra C s (scrubber) as leveraging the company’s proven

scrubber capabilities for WLP and extends them to foundry IC processing. Its soft brush uses precise pressure control to remove particles following wafer frontside, bevel and backside cleans. The tool features an advanced dual-fluid (gas and liquid phase) spray cleaning technique; it can also be equipped with ACM’s patented space alternated phase shift (SAPS) megasonic technology for customers requiring further, more intense cleaning to remove smaller particles. The modular system can be configured with eight chambers for 300mm IC applications – four each for frontside and backside cleaning. The scrubber is highly cost effective due to its flexibility, small footprint and high throughput.




ACM Research
Ultra C Scrubber

When announcing its new cleaning systems, the company also stated that it was adding its Ultra Furnace to the product lineup. According to Wang, this tool is a ‘broad platform’ for ACM’s entry into dry processing applications. “This opens another large market for ACM beyond wet processing. In our view, innovation in vertical furnace technology is required for the industry to progress to more advanced manufacturing nodes. That is why ACM entered the market. We have been hard at work on the furnace for more than two years. It is a joint development project of our world-class technology teams in China and Korea.”

“The two teams developed a new hardware platform that combines our proven stable software and proprietary control system. The Ultra Furnace delivers reliable control of pressure, gas flow-rate and temperature; it is optimized to deliver high performance batch processing of up to 100, 12-inch wafers. It initially supports low-pressure chemical vapor deposition processes, or LPCVD. With additional development work, the furnace tool can be expanded to address oxidation, annealing processes, and future atomic layer deposition processes. We delivered our first Ultra Furnace demo tool to a key customer in the first quarter, and expect qualification by the end of this year,” Wang noted.

Thanks to ongoing growth, the company broke ground 7 July on a new facility in the Lingang Special Area of the China (Shanghai) Pilot Free Trade Zone, about 30 miles from the company’s China subsidiary headquarters. The new facility will consist of a 100,000 square meter factory with R&D facilities. The company has already begun construction, targeting a ramp to initial production in the second half of 2022.



Implementing smart manufacturing in the sub-fab through operational excellence

Silicon Semiconductor recently explored methods for implementing smart manufacturing and Industry 4.0 concepts in the sub-fab through a webinar presented by Edwards Vacuum. Given the timeliness of the subject during the COVID-19 pandemic, Edwards was invited to capture essential webinar details in an article timed for SEMICON West 2020.

BY EDWARDS VACUUM

SILICON SEMICONDUCTOR recently hosted a webinar on the application of smart manufacturing and Industrie 4.0 concepts in the semiconductor manufacturing sub-fab. The webinar was presented by Edwards Vacuum; Silicon Semiconductor's technical editor, Mark Andrews, moderated a discussion among Edwards presenters: Alex Smith, vice president of field operations and safety; Alan Ifould, head of marketing and business transformation, and Neil Condon, head of digital solutions. The webinar followed a question and answer format with a central theme of exploring

the ways smart manufacturing in the sub-fab enables smart manufacturing in the cleanroom. Edwards, a leading provider of vacuum and abatement systems for the semiconductor industry, describes their approach to implementing smart manufacturing in the sub, a program they call Operational Excellence. With over 100 years of rich heritage, Edwards has served the semiconductor industry since its birth and has installed over 100,000 vacuum pumps and 10,000 abatement systems. Following is a condensed version of the webinar content.

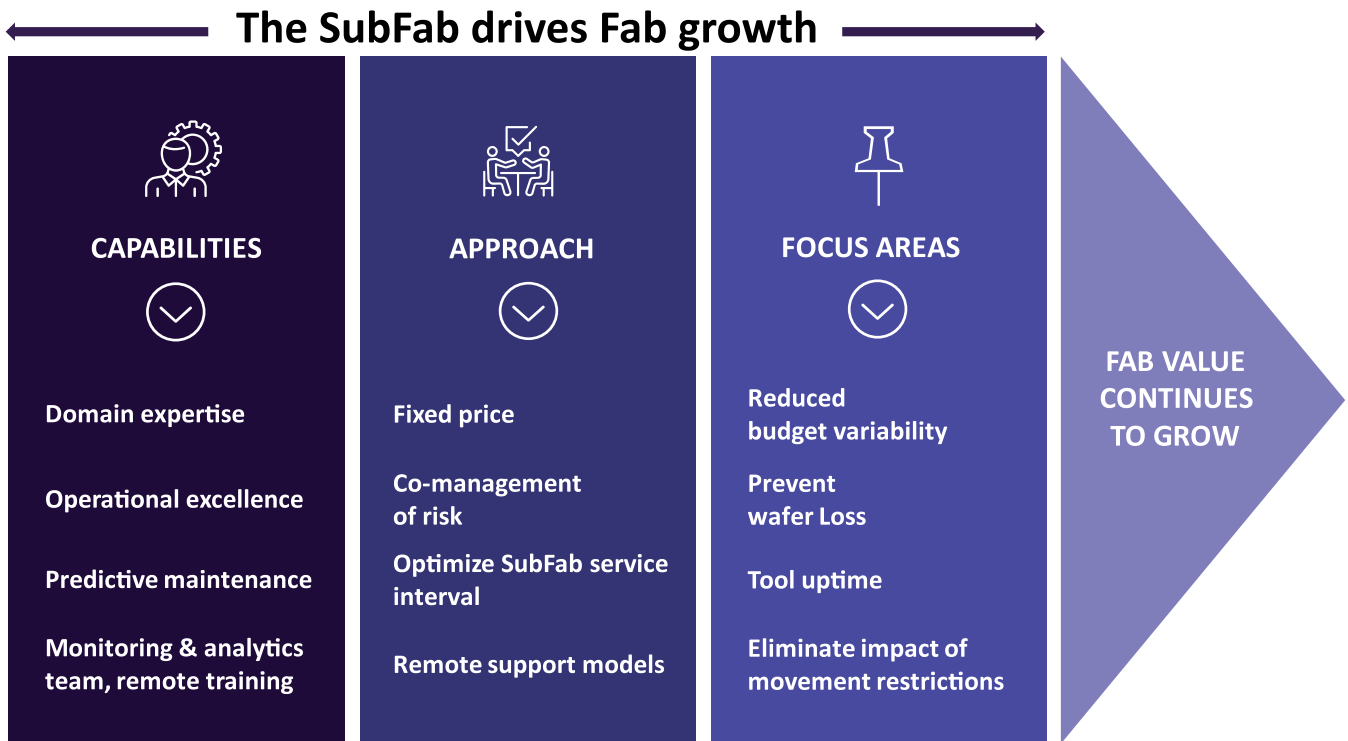


Figure 1: The SubFab can drive fab growth through domain expertise, operational excellence, and predictive maintenance combined with monitoring and analytics to yield many benefits including increased uptime and reduced overall costs.

Smart manufacturing/Industrie 4.0

MODERATOR: Is there more to smart manufacturing than simply collecting more data? What is Edwards approach?

EDWARDS: Smart manufacturing is about much more than simply collecting more data. It is about how the data is used. At Edwards we talk a lot about Operational Excellence – a term we use to describe our model for continuously improving our business operations. It is our way of effectively integrating people, machines, and processes to co-manage risk and deliver outcomes our customers care about. Data drives the process but is useless without domain expertise, the collective individual and institutional knowledge that transforms data into actionable insights. Domain expertise finds the solution.

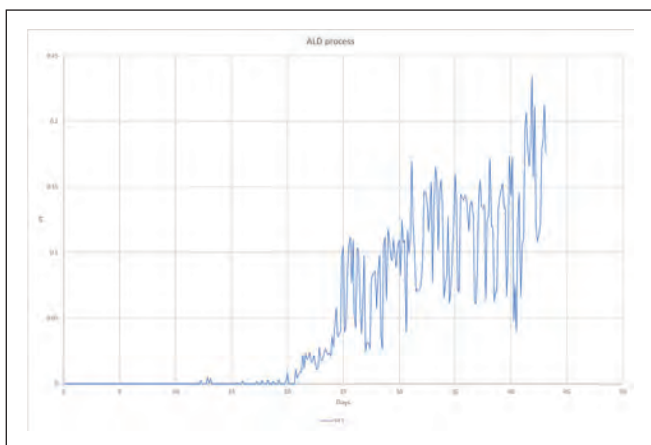
Operational Excellence drives adoption – throughout our own and our customers’ organizations. For example, we might collect more data about performance so that we can detect an under-performing system earlier and, with our customer, plan the right service intervention. That could be moving a pump exchange forward, to avoid unplanned-downtime on a critical tool; or refining a planned maintenance schedule to lengthen intervals and use fewer consumables and spare parts; or triggering an investigation to understand whether a different combination of product and service offerings would deliver better performance. We also use data about the performance of our service teams, and the procedures they use, to adjust procedures and

drive training programs. We apply lean principles with a framework we call VTPS (vacuum technique production system) that tracks things like workplace organization, inventory management, adherence to well-designed work standards, and the idea of “Right from me”, which underpins a culture of principle-driven leadership, safety and continuous improvement.

MODERATOR: What market need does Edwards’ technology, software & in-the-field service expertise address?

EDWARDS: A fab is an expensive tool, and down events are disruptive and costly. The impact of disruption is magnified when the supply chain is stressed, as it is now and is likely to remain for the foreseeable future. In spite of pandemic-induced stress on the supply chain and numerous other effects on operational efficiency and consumer demand, our customers have remained resilient. Recovery is underway for many, though variables within the crisis remain difficult to predict and heightened risk and uncertainty appear likely to persist.

In this context, anything we can do to reduce risks and uncertainty in the sub-fab that could affect the cleanroom is critically important. Any activity that reduces downtime, scheduled or unscheduled, can generate large savings. For instance, at one foundry customer we used our advanced data analytics to reduce the number of abatement PMs from 120 per year to 17 per year.



A vibration signal from a pump on an atomic layer deposition tool (left) and a photo of material deposited on internal components (right). Data analysis predicted the likelihood of a tool fault ahead of scheduled maintenance. After removal, a detailed analysis confirmed that the part was indeed about to fail; proactively replacing it prevented unscheduled process downtime and potential wafer scrap losses.

With each PM lasting 6-12 hours and consuming several thousand dollars' worth of spare parts, the cost of parts and lost production ran well over half a million dollars. This was just on one tool. There is much to gain by focussing on sub-fab equipment.

Sub-fab evolution

MODERATOR: How has the sub-fab evolved in recent years?

EDWARDS: As the number of processing steps required by leading edge processes grows, so does the need for vacuum and abatement. A fab that starts 40K wafers per month has thousands of process tools and supporting pumps and abatement systems. Processes have become harsher and more reliant on high quality vacuum. Environmental regulations continue to tighten, meaning the process cannot run without effective abatement.

Even fabs using legacy 200mm processes are changing. Many use a mix of refurbished 200mm tools and expensive hybrid solutions – 300mm tools adapted for 200mm wafers. The mix of old and new can introduce complexity into the sub-fab support infrastructure as well as the clean room. Against this backdrop, maintaining productivity through these strategic investments is essential to maximizing ROI and profitability. So overall, we see more costly consequences for safety excursions and unplanned vacuum and abatement down events across all sectors. The sub-fab is now regarded as a key opportunity for effectivity improvements. In response to these challenges, sub-fab equipment has evolved to be more sophisticated and tightly controlled while recruiting and retaining staff with the appropriate domain expertise has become more difficult. Within Edwards we recognized a clear need to develop a program to share and embed domain expertise, and ingrain cultural behaviours that assure safety, consistent performance, problem ownership, personal

growth, and reward. This was the initial driver for developing our model for Operational Excellence, which focuses on creating teams, technologies and cultures that can continuously contribute to improved tool availability and reduced risks.

MODERATOR: What is the cost of failure when sub-fab systems suffer unplanned downtime?

EDWARDS: It is hard to be specific about costs of failure as every fab has their own assessment and accounting methods. We base our models on assumptions that we test with customers in different sectors. Costs can vary widely. If a seal fails and toxic gases escape, the whole fab may be evacuated. An unplanned vacuum fault on a batch furnace can risk losing 125 wafers valued at several hundred thousand dollars. A faulty abatement system may cause a tool to be offline for several hours. Planning and anticipation are key. A vacuum pump fault can typically be rectified in around 4 hours, by swapping the pump. But if the tool is brought down in an uncontrolled manner, chamber components may be required, or even a complete requalification lasting up to 72 hours, plus all the costs of disrupting production.

Sub-fab systems approach

MODERATOR: Given the complexity of vacuum systems, how do major components interact, affecting uptime & fab performance?

EDWARDS: There are many examples of inter-dependencies among components of a vacuum process tool. Focus often falls on the pump itself where pressure can vary by several orders of magnitude and temperature can change by hundreds of degrees. But we also frequently see pumps that have stopped because a leak several meters upstream drove a chemical reaction in the pump.

Sometimes there seems to be a responsibility no-man's land between the pump and the chamber,

which makes these issues hard to track down. To find the root-cause of a problem you need to examine the system as a whole, from the chamber through to the exit from the abatement system, and sometimes the supporting facilities as well. The key to progress here is collaboration. When all the stakeholders and domain experts work together, it is much easier to get to the root-cause, and implement a solution that delivers consistent performance and reliability.

In one case, a customer had a tool that was delivering only 10% of the productivity of peer tools. Our primary predictive analytics indicated the performance of the vacuum pump and supporting abatement systems degraded over an unusually short period of time, and at an increasing rate. This behaviour pointed to wider influences. Other signatures we saw in the data pointed to a fault upstream of the vacuum pump. When the customer provided critical contextual data from the wider fab, we identified a specific issue in the foreline that occurred around a maintenance activity owned by another team. This is a clear example of how a holistic approach to understanding the vacuum system is so important. The key here was being able to add context to what the data analytics showed. We get that context by drawing on our own domain expertise in how our equipment is known to behave. In the end we collaborated to create new maintenance procedures that assured a robust vacuum system and tool throughput returned to normal.

MODERATOR: Manufacturing ICs is complex; processes are tweaked, sometimes daily: How does Edwards determine what is useful for improving sub-fab performance?

EDWARDS: There are two sides to this. The first is the equipment itself. It needs to be configured and setup correctly. Edwards makes a lot of different product variants, and all of them can be tuned or configured through software. For example, our iXH dry pump for harsh CVD and ALD processes comes in 116 variants. The other consideration is the customer's process. Understanding how gases, vapours and by-products interact in the product is key to product selection and configuration. This is our domain expertise and it is the key ingredient that helps us measure and improve performance.

We do that by using Operational Excellence to continuously improve our best-known-methods (BKM) – documents and procedures that specify:

- the right combination of products for the process, *together*, as a system
- the best configuration of those products – where do you put the knobs on those products?
- and the right service and maintenance regime, which is made “smart” by live data about performance.

These BKMs are a global view of what works, a view that we are uniquely qualified to provide by our broad experience with customers and processes across the

Edwards makes a lot of different product variants, and all of them can be tuned or configured through software. For example, our iXH dry pump for harsh CVD and ALD processes comes in 116 variants

industry. They are getting more and more precise, and, as wafer processing becomes more complex, the relationship between process and BKM is becoming more and more critical.

Sub-fab optimization – Edwards role
MODERATOR: What differentiates Edwards' ability to help manufacturers optimize performance, reduce downtime, gain greater consistency, and reduce operational costs?

EDWARDS: When we examine the sub-fab space, we see many excellent companies offering some of the capabilities Edwards has. But we believe our framework for Operational Excellence and our broad domain expertise clearly stand out. We practice what we preach, finding confirmation for that belief in our own data. We have operations in locations around the world, each at a different stage in its journey toward Operational Excellence. When we compare performance metrics based on customer outcomes for each facility, we see a clear correlation between performance and the maturity of their journey. It is important to note that most of the improvement arises from effective use of all the disciplines in the Operational Excellence model, not just the use of data analytics. This is why we believe that, in the sub-fab, smart manufacturing must adopt a holistic approach to the effective interaction of people, machines and processes.

Safety

MODERATOR: Safety is a key metric for any fab operation. But how does continually collecting and analysing operational parameters improve safety while increasing uptime?

EDWARDS: We have all experienced the difference in being able to plan and make time for a task versus that feeling of being rushed to complete something against a deadline. Under pressure, methods may be improvised and risk-assessments rushed. Safety becomes reliant on the least reliable controls, i.e. personal protection equipment, procedures, and signs. These kinds of controls should be the last

resort, not the first, as they rely on strict adherence and the absence of human error to be effective. It is much better to rely on designed-in solutions for risk mitigation. Equally important, the work performed in rushed conditions with improvised methods is inevitably less consistent, leading ultimately to performance variability and increased downtime. Using operational parameters to predict events provides the advanced warning needed to plan a task well.

Trained personnel can be better positioned to follow well-designed, risk-assessed standard processes using tools designed to get the job done safely and correctly. Not only does this encourage safe working practices with known risks controlled, but the consistency of results and equipment uptime can be improved. To achieve this, we collect safety data and maintenance data alongside operational parameters. That information informs the design of our equipment, our procedures, and our tools. The more we use data to help us think about the task at the early design stage the better we can design features to reduce risk and improve consistency of performance. Our Operational Excellence safety culture drives this whole safety improvement cycle.

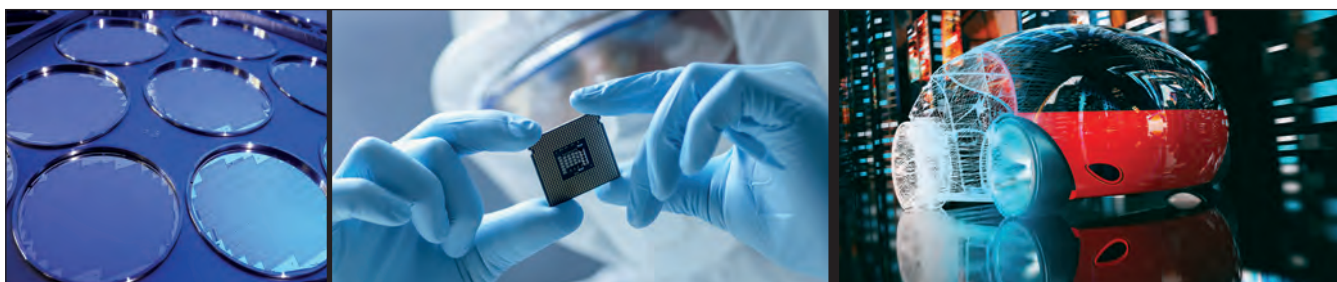
Pulling it all together

MODERATOR: Can you re-cap the Operational Excellence model and its role?

EDWARDS: Our Operational Excellence model is the way we see smart manufacturing coming to the sub-fab: the best way to implement the actionable insight from data analytics and domain expertise. It is our framework to ensure that people, machines, and processes work together most effectively to achieve the best possible performance and the outcomes our customers need.

Like all operational models, it is a framework that collects and integrates many distinct capabilities effectively. We have spoken of many of these in this article. But to correctly define the role of Operational Excellence we must remember its purpose. The role of Operational Excellence is to reduce risk and uncertainty in the sub-fab, and in so doing to increase the value of the sub-fab by reducing overall fab cost. We achieve that by applying capabilities in a structured approach, to solve the problems our customers focus on.

It is not something that Edwards or its employees achieves in isolation. The whole principle of the model is engagement. Our teams are encouraged to own their workplace and run it safely and effectively. As we have discussed, many problems need cross-functional communication to reach resolution. We develop collaborative partnerships with our customers that allow us to manage risk, together.



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Rely on SAM

for 3D package device analysis

The emergence of highly accurate wafer bonding and die stacking has enabled new generations of 3D semiconductors. As stacks grow, so does complexity, which in turn makes reliable, non-destructive inspection and testing critical to high yield and product reliability. PVA TePla Analytical Systems discusses scanning acoustic microscopy (SAM) as a means to ensure scalable, accurate inspection.



THE CONCEPT BEHIND advanced 3D packaging is to vertically stack multiple dies or wafers – the Z-dimension – to achieve better performance with lower power requirements, smaller size and lower cost. However, as 3D packages become increasingly complex, so do the challenges of identifying defects in multiple layers of stacked dies, silicon interposers and interconnections including through-silicon vias (TSVs) as well as fine-pitch micro-bumps.

With less accessibility to internal components and a need to scan multiple, stacked layers, the focus is now shifting to methods of non-destructive testing both in manufacturing and for failure analysis. Non-destructive testing of 3D packages with scanning acoustic microscopes (SAM) identifies defects down to the sub-micron level for 100 percent inspection and failure analysis.

3D advanced packaging

In general, the term 3D packaging applies to products manufactured by stacking (and bonding) silicon wafers or dies and interconnecting them vertically. This covers many integration schemes, including 3D wafer-level packaging, system in package (SiP), package on package (PoP), 2.5D and 3D, stacked ICs and other forms of heterogeneous integration.

To achieve vertical stacking, early 3D packages relied on interconnects such as wire bonding and flip chips. Today, communication between chips often involves a

silicon or organic interposer or bridge, with TSVs. The interposer acts as the bridge between the chips and the board, while increasing the I/Os and bandwidth.

The concept of utilizing chiplets in 3D designs is also gaining momentum for advanced packaging. In this approach, modular chips – or chiplets – from third party vendors are used to build a package or system by stacking the components vertically.

A key benefit of utilizing chiplets to construct a microelectronic system is the ability to select optimized CPU, IO, FPGA, RF or GPU components. Chiplets can be mixed-and-matched using a die-to-die interconnect scheme involving a silicon interposer, a silicon bridge or high-density fan-out. This approach has been embraced by Intel, which recently announced its new Foveros 3D packaging technology that allows complex, heterogeneous logic chips to be stacked directly on top of each other. Intel uses an active interposer instead of a typical passive silicon interposer. As an alternative, Intel is also offering its silicon bridge technology called Embedded Multi-die Interconnect Bridge (EMIB).

The Defense Advanced Research Projects Agency (DARPA), an agency of the US Department of Defense, already plans to develop a large catalog of third-party chiplets for commercial, military and aerospace applications. The goal of DARPA's CHIPS program (Common Heterogeneous Integration and Intellectual

Property Reuse Strategies) is to increase overall system flexibility and reduce design time by as much as 70 percent, according to the agency.

“The vision of CHIPS is an ecosystem of discrete modular, reusable IP blocks, which can be assembled into a system using existing and emerging integration technologies,” writes Andreas Olofsson in program information available from DARPA.

Whether for commercial, consumer or defense-grade components, there are challenges to making the chiplet concept work, including how to verify and test the individual chiplets from a variety of third-party vendors. Integrating multiple chiplets into stacked, 3D packages also requires high-density interconnections, all of which are potential sources of failure.

In comparison to other 3D package types, for example, stacked dies with through-silicon vias (TSV) require much smaller, finer pitch solder bumps that create additional challenges in defect detection. Any defective chiplets in the package will result in a non-functional device even if all other modules are functional.

Given the combined value of the chiplets, interposer and other components, a single defective chiplet or poor interconnection can render the entire 3D package non-functional. This is driving the requirement for 100 percent inspection during manufacturing, ideally with non-destructive testing methods.

Non-destructive testing of 3D packages

Manufacturers taking designs into the third dimension face a number of challenges including the need to perform 100 percent inspection with relatively high throughput to identify and remove 3D packages or components that do not meet quality requirements.

Among the available non-destructive methods, scanning acoustic microscopy is the most widely used techniques for testing and failure analysis involving stacked dies or wafers.

SAM utilizes ultrasound waves to non-destructively examine internal structures, interfaces and surfaces of opaque substrates. The resulting acoustic signatures can be constructed into three dimensional images that are analyzed to detect and characterize device flaws such as cracks, delamination, inclusions and voids in bonding interfaces, as well as to evaluate soldering and other interface connections.

A unique characteristic of acoustic microscopy is its ability to image the interaction of acoustic waves with

the elastic properties of a specimen. In this way the microscope is used to image the interior of an opaque material.

Scanning acoustic microscopy works by directing focused sound from a transducer at a small point on a target object. The sound, hitting a defect, inhomogeneity or a boundary inside material, is partly scattered and will be detected. The transducer transforms the reflected sound waves into electromagnetic pulses that are displayed as pixels with defined gray values thereby creating an image.

To produce an image, samples are scanned point by point and line by line. Scanning modes range from single layer views to tray scans and cross-sections. Multi-layer scans can include up to 50 independent layers. Images from different depths can be combined into a single scan as well, called Tomographic Acoustic Micro Imaging (TAMI).

When higher throughput is required, up to 4 transducers can simultaneously scan for defects. Multiple transducers can be used on a single



PVA TePla Analytical Systems

substrate. In this approach, the images are stitched together – alternately, multiple transducers can simultaneously scan multiple substrates.

“Scanning Acoustic Microscopy provides non-destructive imaging of defects and delaminations in die and package materials,” remarked Lisa Logan, Applications Manager Scanning Acoustic Microscopes for PVA TePla Analytical Systems, a company that designs and manufactures advanced scanning acoustic microscopes for both laboratory and production environments.

“SAM is particularly useful for inspection of small, complex three-dimensional devices,” added Logan. “The equipment is highly sensitive to the presence of delaminations and air-gaps at sub-micron thicknesses.”

The most common defects in 3D packaging are delaminations, substrate cracks, die tilt, misalignment and voids in micro-bumps and other bump defects. Solder bridging, popcorn cracks, and voids in underfill are also common, as are voids and delamination in through silicon vias (TSVs). The resolution of microscopic SAM image depends on the acoustic frequency utilized, the material properties being scanned and the aperture of the transducer. The

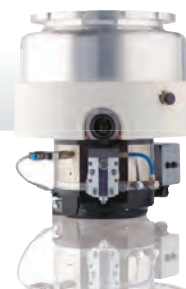
frequency of the ultrasonic signals generated for 3D package inspection is typically within 15 to 300 MHz. Transducers, the heart of all SAM systems, play such a critical role that manufacturers like PVA TePla Analytical Systems designs and manufactures the transducers used in its equipment utilizing a proprietary thin film technology process.

The frequency of the ultrasonic signals can even be increased into GHz range, which makes it possible to detect defects even in the sub-micron-range. PVA TePla’s high-resolution, GHz frequency SAM tool, for example, successfully detects voids in TSVs of 5-micron diameter and 50-micron depth, immediately after plating.

According to Logan, several leading suppliers of programmable logic devices have already evaluated and purchased high resolution SAM equipment for non-destructive analysis of next generation 3D products to scan for packaging anomalies.

“3D chip manufacturers are trying to push the limits on what they can detect, in terms of defects,” says Logan. “So, today the evaluation of scanning acoustic microscopy equipment often comes down to which equipment delivers the highest resolution at fastest throughput speeds for 100 percent inspection.”

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MEMS oscillators:

enabling smaller, lower-power IoT & wearables

SiTimes makes a case for MEMS oscillators versus quartz-crystal-based clocking sources.

BY JEHANGIR PARVERESHI, SR. MANAGER, CUSTOMER ENGINEERING
AND HARPREET CHOHAN, DIRECTOR, MARKETING

THE EXPLOSIVE GROWTH in internet-connected devices, or the internet of things (IoT), is driven by the convergence of people, devices and data across the web. Future growth will be strongly influenced by wearable technology as products transition from the laptop to the pocket to the body. Activity trackers are leading this segment in the number of units shipped per year, followed by smart watches and medical monitors/devices, as well as wearable cameras and smart glasses. These devices are enabled by advancements in MEMS and sensor technology, wireless connectivity and new power savings capability.

Wearable devices leverage new timing technology

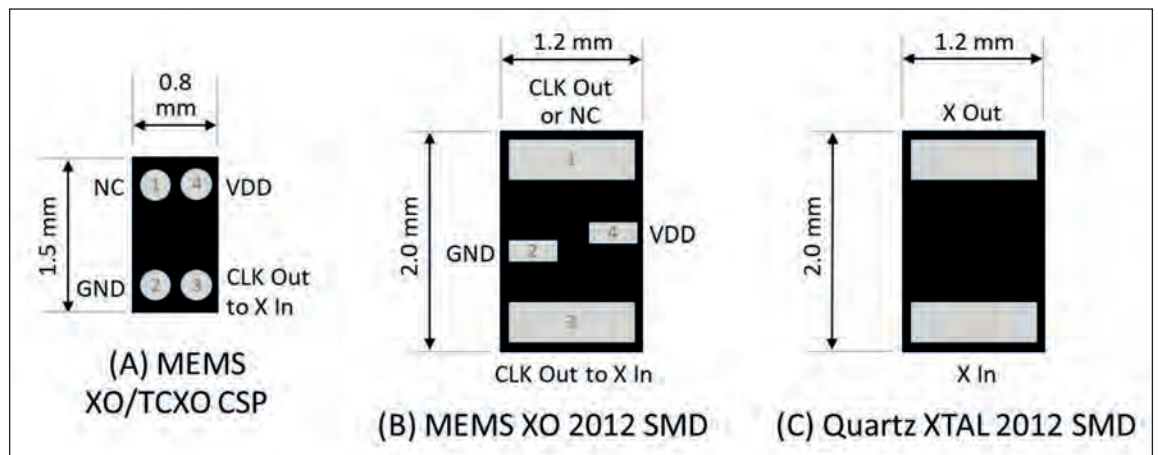
All electronic products require one or more timing devices depending on the processor, partitioning, and various functions in the system. Traditionally,

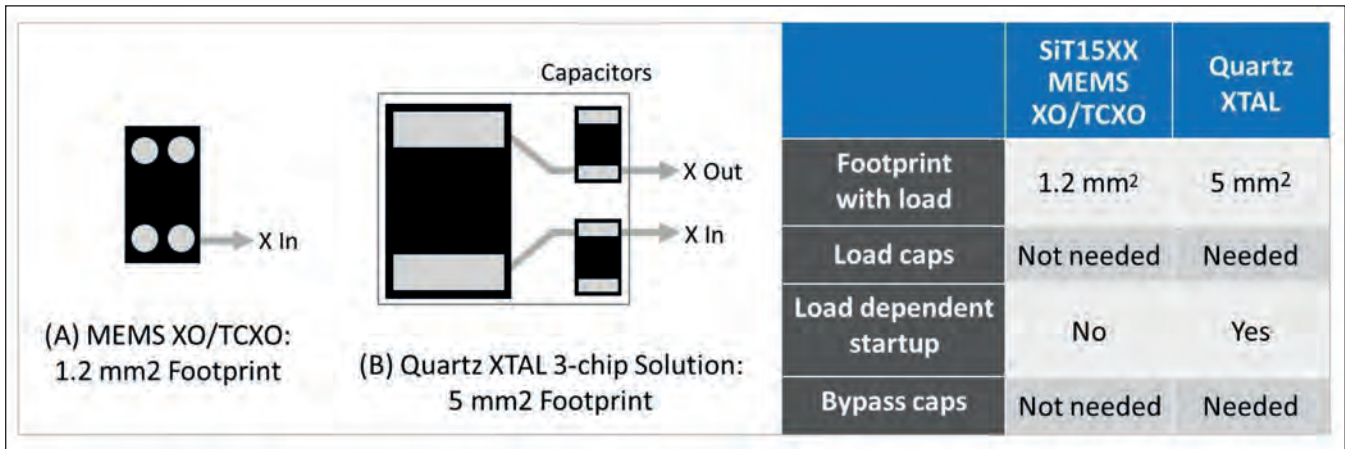
32.768-kHz crystals and low-power MHz quartz-based oscillators have been used for implementing clock functions in battery-powered electronic systems. A new class of ultra-low-power, low-frequency MEMS oscillators now offers advantages over the ubiquitous 32-kHz crystal clock. Innovations in MEMS timing technology is making significant impact in IoT and wearables, especially in the areas of size and power savings.

Key benefits of MEMS timing solutions for IoT and wearables include:

- **Smaller footprint – 80% smaller than quartz**
Smallest 32-kHz oscillator in a 1.5 × 0.8-mm chip-scale package (CSP)
- Oscillator output drives multiple loads, reducing component count and board area
- **Better stability, as good as 3 ppm – translates to higher savings**

Figure 1: Package size and pin location of 32 kHz MEMS XO and TCXO compared to quartz XTALs.





- MEMS XO (oscillator) is 2× to 3× more accurate compared to quartz
- MEMS TCXO (temperature compensated oscillator) is 30× to 40× more accurate
- Better stability means less reliance on network timekeeping updates, longer sleep-mode periods, and 30% to 50% lower power compared to quartz XTAL + SoC oscillator
- Programmable frequency from 1 Hz to 2.5 MHz for sensor interface – enables new architectural options
- More resilient – 50× greater resistance to shock and vibration

All-silicon MEMS timing solutions

Unlike quartz-based devices, silicon MEMS oscillators employ modern packaging technologies. MEMS oscillators consist of a MEMS resonator die mounted on top of a high-performance, programmable analog oscillator IC that is molded into standard low-cost plastic SMD packages, with footprints compatible with quartz devices. To support the space requirements of ultra-small applications, SiTime MEMS oscillators are available in ultra-small CSPs. MEMS oscillators are based on a programmable architecture that allows customization of features including frequency, supply voltage, output swing, and other features.

Miniaturization through integration, smaller package size, and board layout flexibility

SiTime oscillators offer higher integration, new packaging options, and other features that enable size reduction. The SiT15xx 32kHz MEMS timing solutions are designed for replacing traditional quartz crystals in mobile, IoT, and wearable applications in which space and power are critical. These devices are also available in a 2.0 x 1.2-mm (2012) SMD package for designs that require crystal (XTAL) resonator compatibility. SiT15xx 2012 oscillators have power supply (Vdd) and ground (GND) pins in the center area between the two large XTAL pads, as shown in Figure. 1b.

For even smaller size, SiT15xx devices are available in a CSP (Figure. 1a), which reduces the footprint by up to 80% compared to existing 2012 SMD crystal

packages and is 60% smaller than the 1610 (1.6 × 1.0-mm) XTAL package. Another option, as a result of SiTime’s manufacturing processes, is the capability to integrate MEMS resonator die with an SoC, ASIC, or microprocessor die within a package. This option eliminates external timing components and provides the highest level of integration and size reduction. Due to the limitations of crystal resonators, quartz suppliers cannot offer CSP or integrated solutions.

Unlike quartz crystals, the SiT15xx output drives directly into the chipset’s XTAL-IN pin, eliminating the need for output load capacitors, as shown in Figure. 2. Because the oscillator can drive clock signals over traces, it does not need to be placed adjacent to the chipset. This feature, combined with the ultra-low profile (0.55-mm height), enables flexibility in board layout and additional space optimization. In addition to eliminating external load capacitors, SiT15xx devices have special power supply filtering that eliminates the need for an external Vdd bypass-decoupling capacitor, further simplifying board design and miniaturization. Internal power supply filtering is designed to reject noise up to ±50 mVpp through 5 MHz.

Figure 2: Total footprint of 32 kHz MEMS XO and TCXO compared to quartz XTAL and required capacitors.

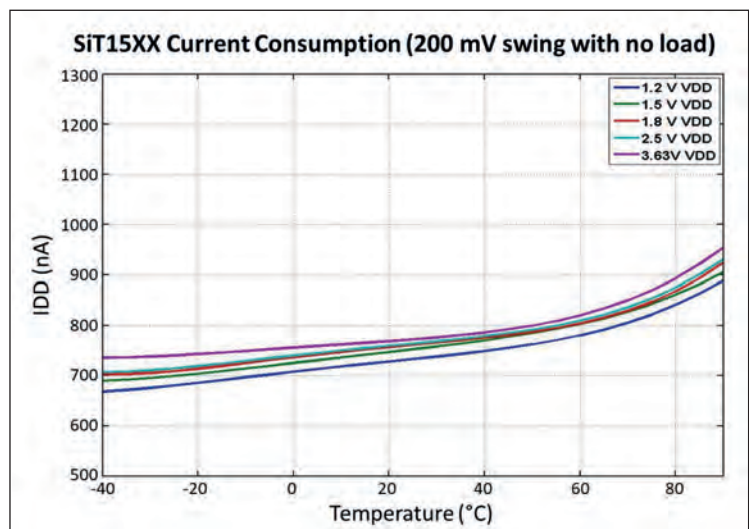


Figure 3: SiT15xx draws less than 1µA over supply and temperature.

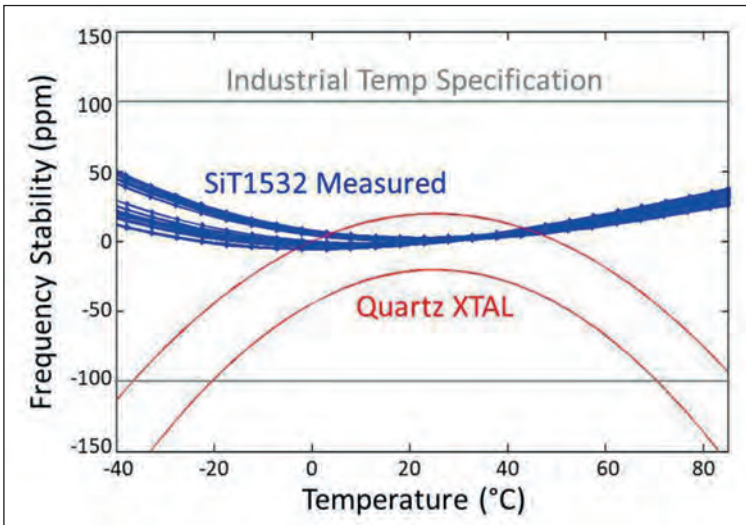


Figure 4: SiT1532 MEMS XO frequency stability compared to quartz XTAL –160 to –200 ppm over temp.

Extended battery life through low current consumption

Low frequency, low power 32-kHz timekeeping devices are widely used in mobile devices where the device is continuously ON for time keeping or controlling sleep modes. These low frequency oscillators are also used to time events such as monitoring and control functions in a power management IC (PMIC) used in battery-powered devices or to perform short system wakeup for timing reference synchronization.

Traditionally, systems generate the 32-kHz clock signal by connecting a tuning fork type or AT-cut quartz crystal to an on-chip pierce oscillator circuit. These quartz time-keeping oscillators are always ON and continuously drawing a few microamps. SiTime’s SiT15xx 32-kHz MEMS oscillators draw less than a microamp of current and can run off a range of regulated or unregulated supply voltages, from 1.2 to 3.63 V. Figure. 3 plots a SiT153x oscillator drawing less than 1- μ A oversupply and temperature.

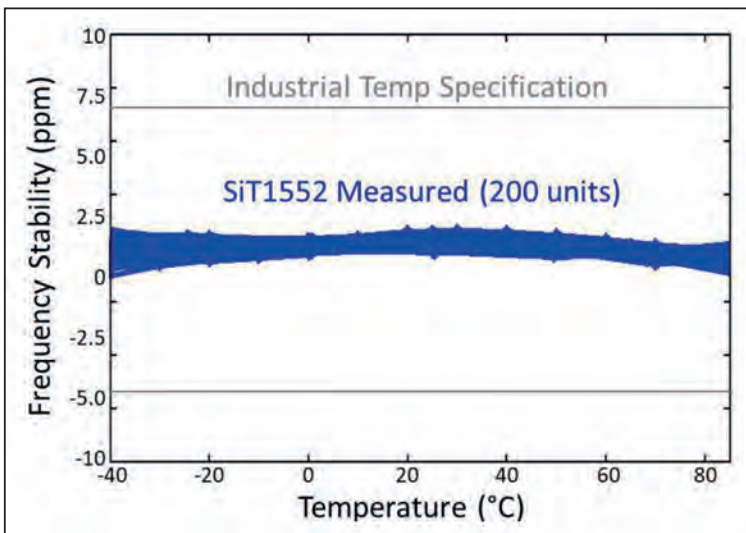


Figure 5: SiT1552 MEMS TCXO frequency stability is 30 to 40 times more accurate than quartz XTAL.

Measured frequency stability

32-kHz MEMS timing devices have a temperature coefficient that is extremely flat across temperature compared to quartz crystals as shown in Figure. 4. The SiT15xx oscillators are calibrated (trimmed) to guarantee frequency stability to less than 10 ppm at room temperature and less than 100 ppm over the full –40°C to 85°C temperature range. In contrast, quartz crystals have a classic tuning fork parabola temperature curve with a 25°C turnover point as indicated by the red lines in Figure. 4.

Figure. 5 plots the frequency stability of 32-kHz MEMS TCXOs. In these devices, the temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32-kHz TCXO with less than 5-ppm frequency variation over temperature. This low level of frequency variation results in extremely accurate clocks that translate to significant power savings. With higher accuracy, wireless systems are less reliant on network

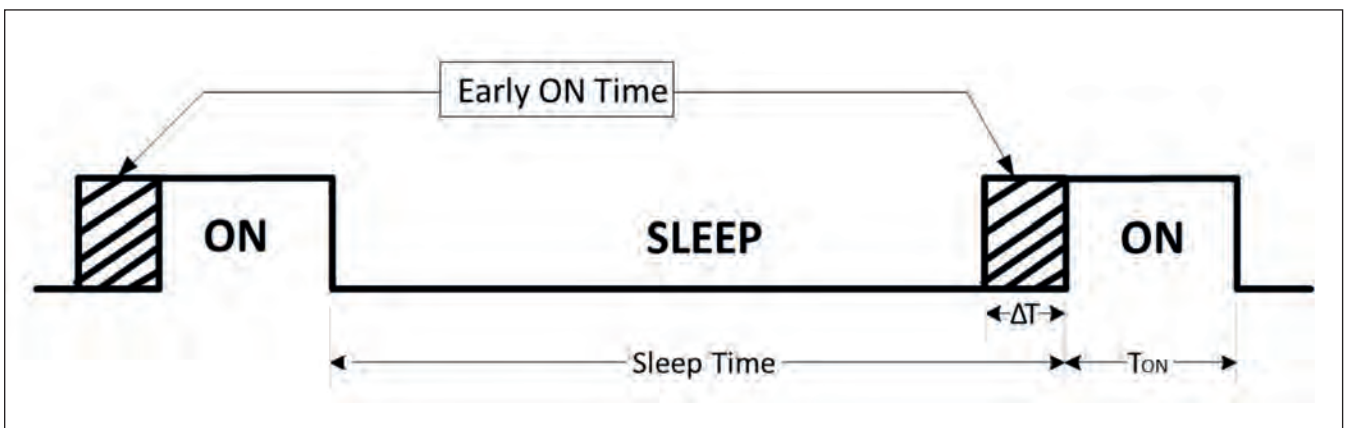


Figure 6: Early ON time (or window widening) is affected by clock accuracy and causes a power penalty.

Sleep Clock Accuracy	Sleep Interval	2 Seconds	20 Seconds	50 Seconds
		Early ON Time		
5 ppm		0.01 ms	0.1 ms	0.25 ms
50 ppm		0.10 ms	1.0 ms	2.5 ms
70 ppm		0.14 ms	1.4 ms	3.5 ms
200 ppm		0.40 ms	4.0 ms	10.0 ms

The table shows that tighter slave clock accuracy reduces early ON time, thereby reducing power consumption.

timekeeping updates and can stay in sleep mode for much longer periods of time.

Extended battery life through better frequency stability
Frequency stability, the clock's stability over voltage and temperature, translates to power conservation. Many mobile and IoT devices reduce power consumption by shutting down the functional blocks with the highest current drain when inactive. However, the system must wake up and periodically communicate with the network. Higher frequency stability allows the device to stay in its low-power state, or sleep state, for longer periods, resulting in significant power savings.

Many wearables continuously collect data and compress and upload it to the cloud via an internet hub device such as a smartphone. This upload is

transferred in short bursts that last a few milliseconds and then the device goes to sleep to conserve power. The cyclic sleep scenario is typical of battery-powered devices in which the device core is shut down for a pre-set time called "sleep time," typically in the range of two to 10 seconds, and awoken when it needs to transmit data during a short burst. The connection event is the "ON" time during which certain functional blocks of the device wake up and stay active for short periods.

Power consumption is proportional to the ratio of "ON" time to the time that devices spend in the "sleep" state. And the sleep clock accuracy (SCA) of the 32-kHz clock that is used to time the sleep state has a direct impact on the battery life. Sleep clock inaccuracies cause the radio receiver (RX) to turn on earlier and stay on longer to avoid missing packets

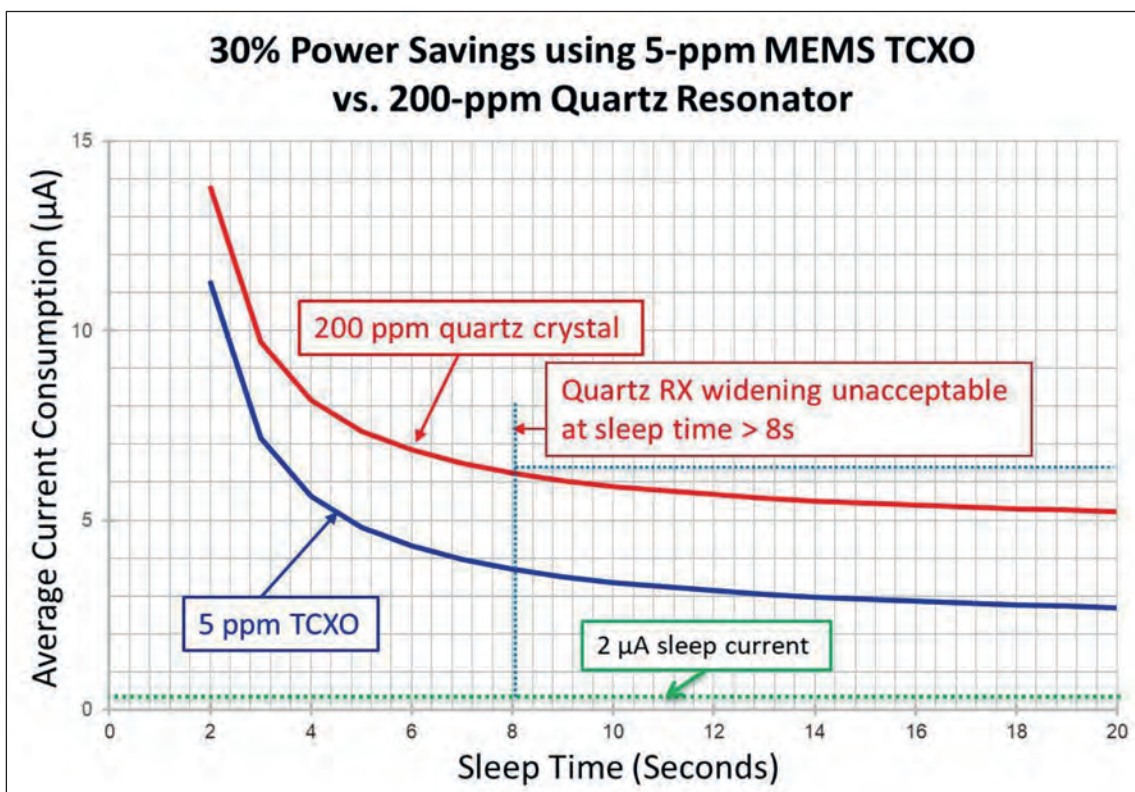
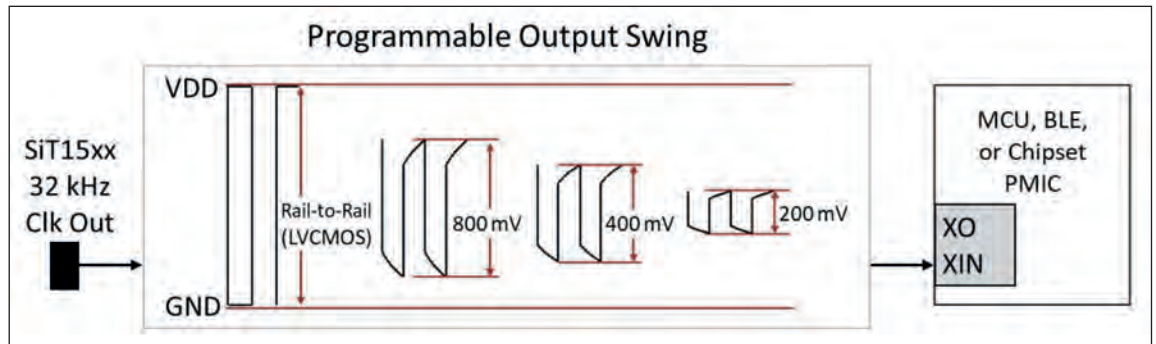


Figure 7: Power savings through use of MEMS TCXO compared to quartz XTAL resonator.

Figure 8: Unique NanoDrive output swing is programmable down to 200 mV to minimize power.



from the master. Clock inaccuracy, measured in ppm, extends early ON time (T), as shown in Figure. 6: $T = (SCA) \times (SLEEP\ TIME)$.

MEMS-based TCXOs, such as the SiT1552, with less than 5-ppm frequency variation over temperature, is a much more accurate alternative than quartz crystals. This accuracy reduces early ON time and allows the system to stay in sleep mode longer. Using a SiT1552, system designers can leverage compression and transmit data in short bursts only when required while keeping the device in its lowest-power sleep state for extended periods and potentially achieve up to twice the battery life.

Figure. 7 shows 30% power savings gained through using a 5-ppm 32-kHz TCXO compared to a 200-ppm 32-kHz quartz-crystal resonator. Shown are two plots of the average current consumption over 1 connection interval for various sleep times ranging from 2 seconds to 20 seconds. These per-cycle average values are computed from a BLE SoC sleep current of $1.8\ \mu A$, a radio receiver power of 9.3 mA, a transmit power of 9 mA, and an average ON-time base-band processing current of around 5 mA.

Extended battery life with programmable features
The analog oscillator IC in SiT15xx devices supports several functions, including a low noise sustaining

circuit, an ultra-low-power precision PLL, and an ultra-low-power programmable output driver. The fractional-N PLL with sub-hertz resolution is used for device calibration and frequency programming from 2.5 MHz down to 1 Hz. The capability to lower output frequency significantly reduces current consumption. Quartz XTALs, due to the physical size limitations of the resonator at low frequencies, do not offer frequencies lower than 32.768 kHz. With lower-frequency options, the SiT15xx family enables new architecture possibilities in battery-powered applications in which the reference clock is always running

Unlike standard oscillators, SiT15xx oscillators can function in tandem with the on-chip 32-kHz oscillator circuit via the oscillator's highly programmable output driver. The output driver can generate various common-mode voltages and swing levels to match different implementations of the on-chip 32-kHz oscillator circuits, as shown in Figure. 8. This output swing is factory-programmable from full swing down to 200 mVpp for the lowest power. The ability to reduce output frequency and output driver current significantly reduces the output load current ($C \times V \times F$). See SiT15xx datasheets for load calculation details and examples at <https://www.sitime.com/products/khz-oscillators> and <https://www.sitime.com/products/mpower-oscillators-1-hz-26-mhz>

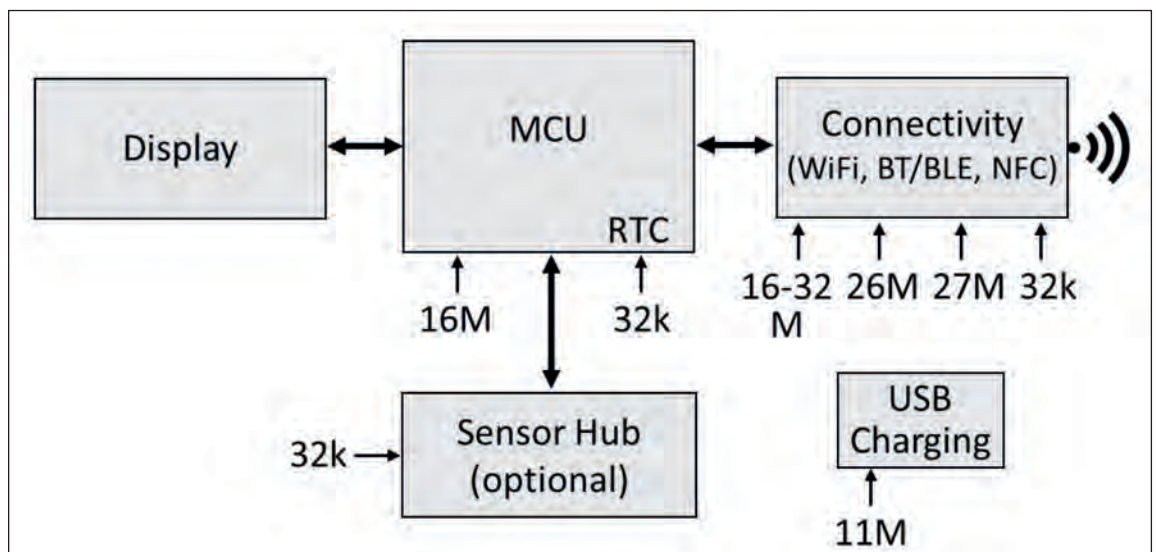


Figure 9: Typical wearable timing architecture.

MEMS are 50 times more robust

By nature of their application, IoT and wearables are used in a variety of environments and can be subjected to frequent and extreme mechanical shock and vibration. When operating in harsh environments, quartz oscillators will degrade and not conform to datasheet specifications. Some quartz oscillators are especially sensitive to sinusoidal vibration and shock and will exhibit significant frequency variation. The SiT15xx device architecture lends itself to higher reliability and resiliency to harsh environmental factors relative to their quartz counterparts. The very small mass (1,000 times smaller than quartz resonators) and structural design of SiTime resonators make them extremely immune to external forces such as vibration and shock. For more details on the resiliency and reliability of MEMS oscillators, see technology paper at: https://www.sitime.com/sites/default/files/gated/AN10045-SiTime-Resilience-Reliability-MEMS-Oscillators_0.pdf

Application and design examples

In the wearable market, products are increasing in functionality while, at the same time, they must consume less power and space. 32-kHz MEMS timing solutions can be used for true pulse-per-second (pps) timekeeping, RTC reference clocking, and battery management timekeeping to lengthen battery life and shrink footprint.

Figure 9 shows the clocking needs in a typical wearable device. A low power 32-bit MCU runs off of a 16-MHz crystal to clock the core and peripherals, and a 32-kHz crystal is used for real-time clocking. The MCU sends data to a connectivity chip that runs off of a 32-kHz crystal used for sleep clock timing.

Figure 10 illustrates a design in which a programmable 1-Hz to 32-kHz SiT1534 MEMS oscillator is used for the sensor application and a 32-kHz MEMS SiT1532 reference clock drives the RTC in an MCU. In this design, the board space is reduced to less than half through use of 1.5×0.8 -mm CSP oscillators.

Figure 11 shows an architecture in which a 32-kHz timing solution is required for two chips: a reference clock for the microcontroller and the sleep clock for the Bluetooth chip. In this design, a single MEMS timing device in a tiny 1.5×0.8 -mm CSP, drives two loads and replaces two 32-kHz quartz XTALs. The footprint is eight times smaller than a design that uses two quartz XTALs in 2012 SMD packages plus the four required load capacitors. This design also saves significant power with 100-times-better stability of an SiT1552 TCXO compared to the BLE chip's internal 32-kHz RC over temperature.

Summary

Innovation in the rapidly growing wearable and IoT segments is fueled by advancements in underlying technologies. MEMS timing technology is one of

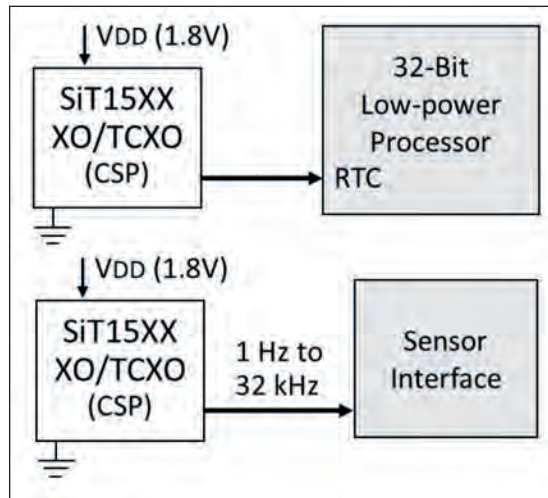


Figure 10: Fitness device timing shown in example 1.

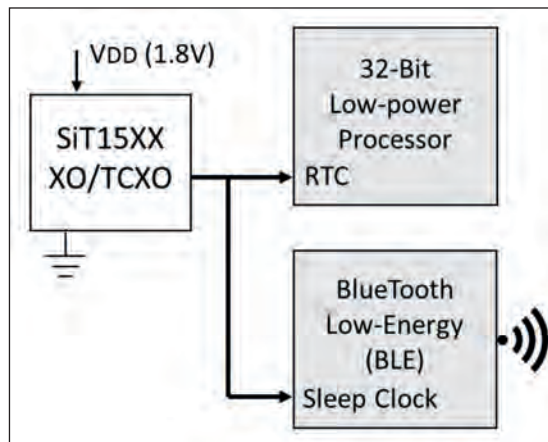


Figure 11: Fitness device timing shown in example 2.

the key supporting technologies enabling the trend toward smaller size, lower power, and increased robustness.

MEMS timing reduces footprint through:

- Smaller, unique packages
- Higher integration that reduces component count
- Board layout flexibility

MEMS timing reduces power consumption through:

- Lower core current draw
- Higher frequency stability that enables longer sleep states
- Programmable frequency
- Programmable output swing voltage

MEMS timing increases robustness through:

- Greater resistance to shock and vibration error

MEMS XOs/TCXOs offer an alternative to the bulkier, less-accurate quartz-crystal clock sources used in past designs. As the IoT continues to expand with increasingly smaller battery-powered devices, low-frequency MEMS-based devices will provide the optimal timing solution and enable new products that were not previously possible.

Structural defects in TO-220

Ultrasound and X-ray work together to image and evaluate harmless anomalies and potential field failures in a TO-220 package.

BY TOM ADAMS, CONSULTANT, NORDSON SONOSCAN

LAUNCHED by an ultrasonic transducer, a pulse of ultrasound travels through the plastic package of an electronic component at a speed around 3,000 m/s. If it strikes a material interface, there are two possibilities: a) if the interface is between two solids, a portion of the pulse will be reflected back to the transducer and another portion will cross the interface;

or b) if the second material is air, the pulse is almost entirely reflected, and none crosses the interface. The second possibility is useful because most of the internal structural anomalies and future field failures in a component result from cracks, delaminations, voids or other gaps containing air. A few defects that are imaged do not involve air - a tilted die, for example, or a missing solder bump, but both types of interfaces can be located and analyzed by ultrasound.

A TO-220 device like the one discussed in this article is designed to be mounted by its tab onto a heatsink in order to dissipate large amounts of heat. Internally, wires run from the die, which is mounted on the substrate, upward to the electrical lead posts. The purpose of acoustic micro imaging of this TO-220, carried out by a C-SAM® tool from Nordson SONOSCAN, was to evaluate interfaces for structural defects: the die attach, the bonding of the wires to the die, and the bonding of the wires to the top of the post. A question that could not be resolved by ultrasound was handled by an X-ray tool.

For acoustic imaging, the TO-220 was first flipped over to image the die attach through the metal back side tab, then turned upright to pulse ultrasound through the encapsulate to image first the die face and second, at a higher plane, the top of the post to which the wires were attached.

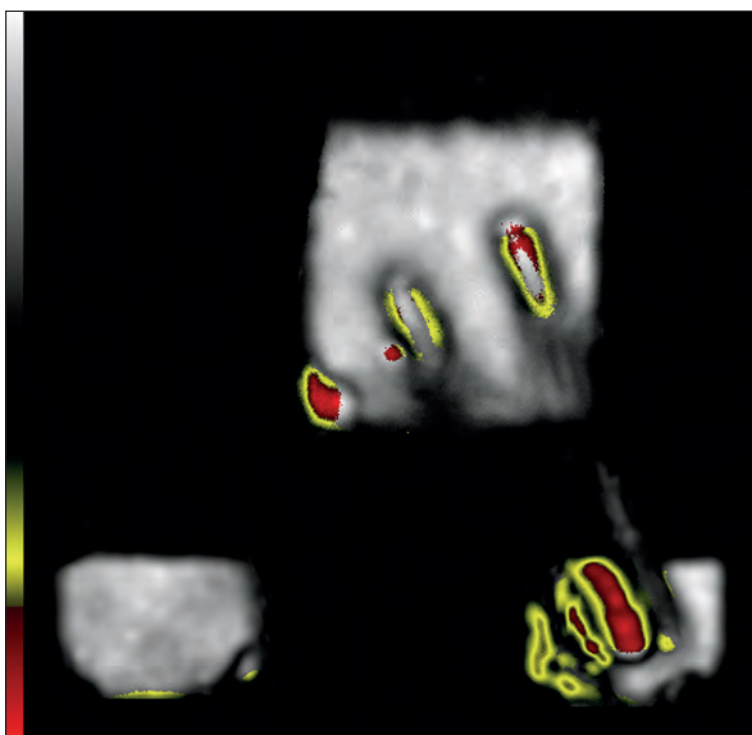


Figure 1: Acoustic image made through the mold compound and showing the die at top and the two posts

At each site, the transducer scanned back and forth a few mm above the area of interest, each second launching thousands of ultrasonic pulses and receiving their return echoes. The echo from each x-y scanned location becomes one pixel in the acoustic image of that area.

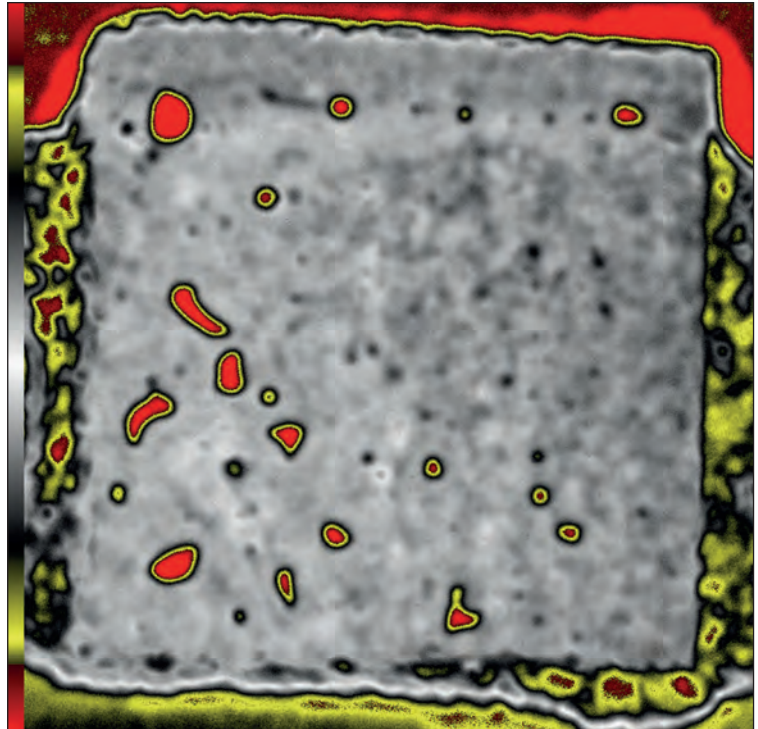
From each returning echo the following information is gathered: the echo's acoustic frequency, its amplitude, its polarity, and the depth from which it was reflected. In these images, the colors report amplitude and polarity.

An acoustic image of all three elements in the package is shown in Figure 1. The vertical distance between the die and the posts is too great to be within the same focus. Figure 1 is therefore made from parts of two acoustic images, one focused on each of the two depths within the package.

The right lead attached to the die at top has a very small red area, but the wire bond area is essentially intact. The red area at the lower left corner of the die, however, is a void that could grow with repeated thermal cycles and cause wire bonds to break. Whether this void is enough to cause rejection of the part depends on the application. It might be suitable in a commercial application, but perhaps not in a military application.

The two wires visible on the die clearly run to the post at the right. There is no indication in this view of wires running to the left post. In this case the wire has a very fine diameter and is too small to be resolved at the low ultrasonic frequency needed to penetrate the mold compound. There is, however, a faintly brighter area on the left post that somewhat resembles a bonded wire.

The back side of the die (Figure 2) was imaged through the metal substrate, to which the die is attached. The variously shaped small red features within the area of the die are voids - red here indicates that there is air in the voids. There are no truly dangerous features such as very large delaminations, or voids close to the corners of the die. The voids cover, in total, about four percent of the die area. The TO-220 package is designed to remove large amounts



of heat swiftly, so these relatively small well-spaced voids in the die attach may pose little threat. The problem area in this component, as can be seen in Figure 1, is the right lead post and the wires attached to its top. The red areas are likely voids, but their exact placement and relative danger must be sorted out. To do so, two different imaging modes were used.

The first was a mode that can, during a single scan, image multiple progressively deeper thin slices of the sample being viewed. At each of the thousands or millions of x-y locations in a given image, ultrasound may be reflected from a single interface, or from multiple interfaces at various depths.

To avoid depth confusion, each image is limited to echoes arriving within a specific time that matches a vertical extent within the part. For the right lead post, a total of 6 gates was defined and imaged, each 600 microns in vertical extent. The echoes from each gate became a separate acoustic image.

Figure 2:
Die attach, as imaged through the bottom of the package

At each site, the transducer scanned back and forth a few mm above the area of interest, each second launching thousands of ultrasonic pulses and receiving their return echoes. The echo from each x-y scanned location becomes one pixel in the acoustic image of that area

Nordson Sonoscan

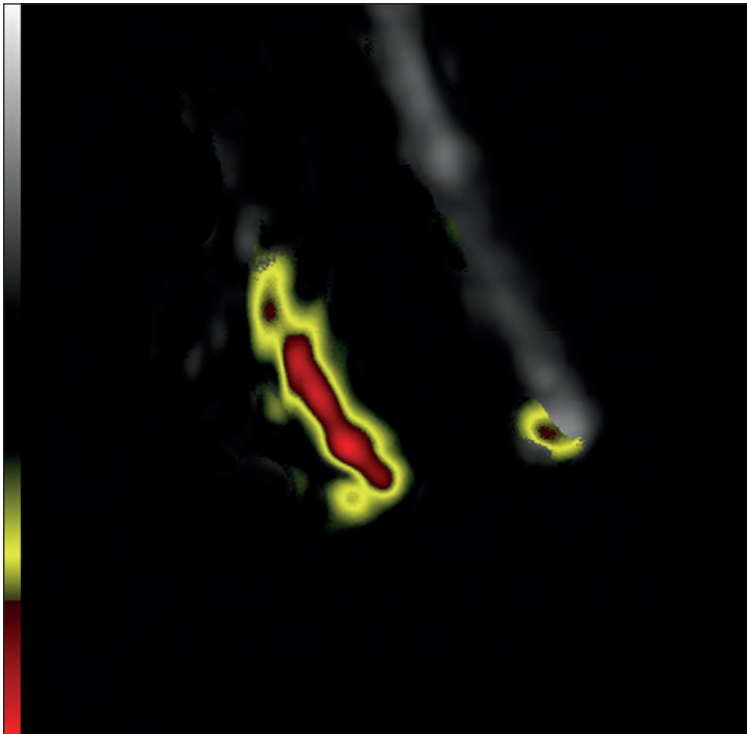


Figure 3: The two wires attached to the right post. Red areas are anomalies

Of the six gates, only gates 3 and 4 revealed details of the two wires and their attachment to the post. In gate 3 (Figure 3), the wire at right is faintly visible. It has no anomalies at this depth except for a small void at its termination. The wire at left has a similar tiny void at its termination, but has a larger void along part of its length.

Gate 4 is seen in Figure 4. The wire at right is very faintly visible. The small void near its tip is visible at this depth. The white area at right is the top of the post to which the two wires are attached. The post extends to the left at least as far as the leftmost void, although it is hidden by overlying features for most of this distance. The large red feature at center is a void, and other voids are scattered about. Red in a delamination or void identifies an area that reflects nearly all of the arriving ultrasound. Red is at the very bottom (=strongest negative echo) in the color map at left. Where the side of a feature becomes steeper and reflects ultrasound less directly in the direction of the transducer, red changes to black. Even steeper sides reflect yellow, the next color on the map.

To get an enhanced view of the interior of this device, it was also imaged with the C-SAM's nondestructive cross-sectioning feature called Q-BAM (Quantitative B-scan Analysis Mode). A line was described on the acoustic image of the top of the package through which cross-sectioning would cut through the area of the two wires bonded to the lead post. The resulting acoustic cross-sectional image is the dimensionally accurate equivalent of a physical cross sectioning made by cutting down through the package along the same line.

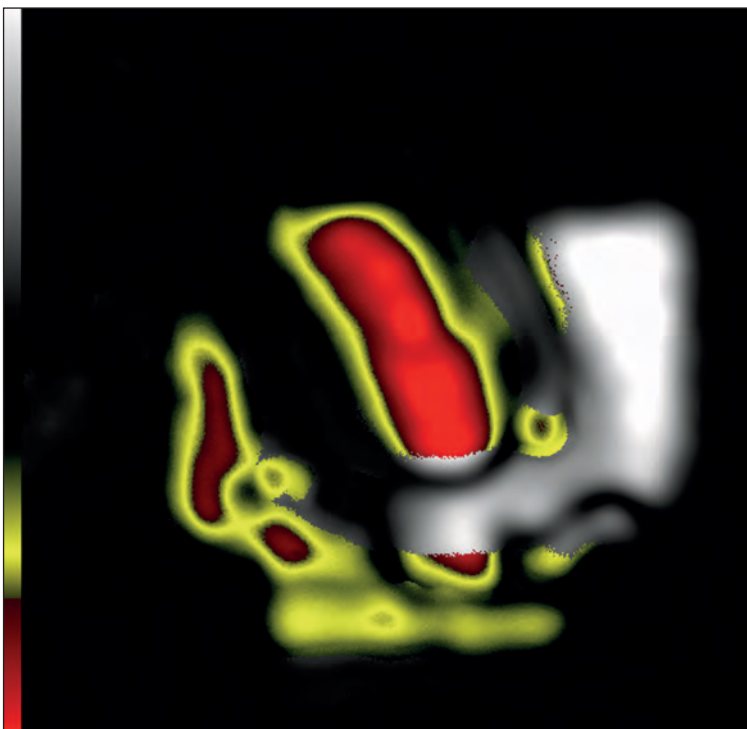


Figure 4: Same view, but in a slightly deeper gate

If the sample were physically sawn open along the same line, the same features would be found in the same locations. A light photograph of the sectioned face would look much like the acoustic cross-section. The concept can also be used in a different manner: before physical sectioning, the sample may be imaged acoustically to spot the location through which the physical section will provide the desired information.

The white horizontal line just below the centre of Figure 5 is the line along which the transducer scanned this component in order to produce the acoustic cross-section in the top portion of the Figure. On its first pass along this line, the transducer accepted echoes only from a defined thin depth at the bottom of the package just above the post. The transducer was then raised very slightly and scanned back along the line. By the time it reached the top of the package it had collected the echoes needed to produce the acoustic cross-section seen in the top section of Figure 5.

In the sectional view, the surface of the package is marked by a horizontal red line. In the bottom half, the cross-sections of five features are shown running from left to right. Each feature lies directly above its location

on the thicker white line in the top view below. From left to right, these features are:

1. a large air gap on the surface of the post.
2. the left wire and the void on top of it.
3. the large void to the left of the right wire.
4. largely the interface between the mold compound and the post.
5. a void at the top of the post itself.

There is a sixth, rather small feature, apparently a void, directly above

6. #1, just below the package surface.

The acoustic images in Figures 1 through 5, however, do not reveal all the wires extending from the die to the posts. The acoustic images revealed two fairly large wires. Smaller diameter wires would be difficult to see because they scatter most ultrasound away from the transducer. In addition, a smaller diameter wire might be invisible acoustically at low frequencies. If ultrasound is entirely blocked by an air interface, the wires beneath the air gap will not be imaged.

Subsequently a Dage Quadra 7 X-ray system was used to image the TO-220. An X-ray beam is not stopped or even attenuated by an air gap. Imaging was first attempted through the heat sink, but the thickness of the metal was too great. (Ultrasound would have penetrated the metal but would still have been scattered rather than reflected by the round wires.) to get additional information. The TO-220 was therefore X-rayed from the side, a longer route through the much less attenuating mold compound. The results are seen in Figure 6.

Four wires are visible as vague dark lines marked by numbers in the X-ray image. The image colors have been inverted to make the wires more visible. Their precise orientation cannot be discerned, but it seems likely, taking into consideration the very faint features on the left post in Figure 1, that two wires run from the die to each of the two posts.

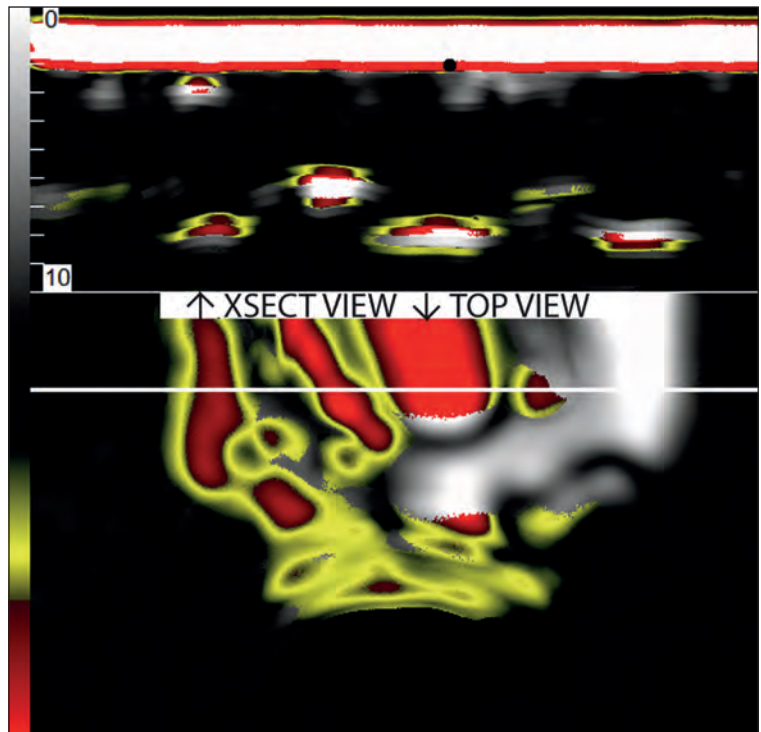


Figure 5: Top portion is a non-destructive cross-section through the horizontal white line below the legend

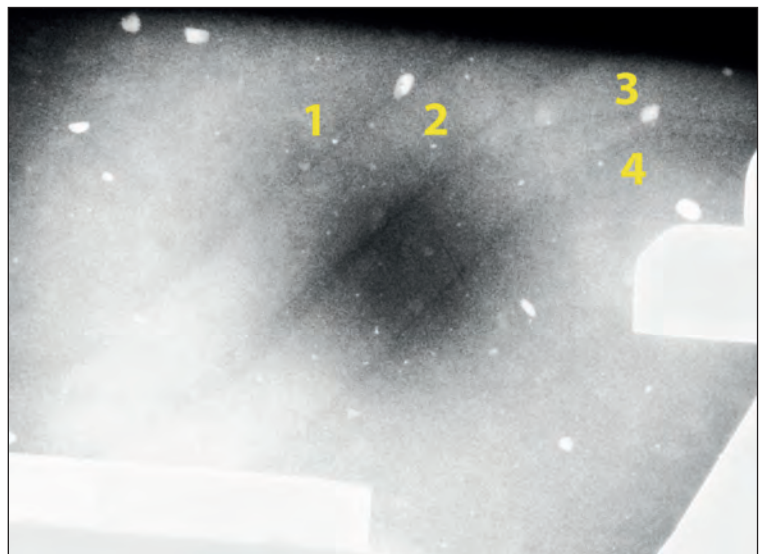


Fig 6: An X-ray beam inserted into the side of the mold compound revealed the four wires

The acoustic images revealed two fairly large wires. Smaller diameter wires would be difficult to see because they scatter most ultrasound away from the transducer

The vertical ferroelectric FET:

a new contender for 3D-NAND Flash memory and machine learning

Jan Van Houdt, Scientific Director at imec, explains how the FeFET works and how this exciting 'newcomer' might fit in the next-generation memory landscape.

FERROELECTRICS are a class of materials that consist of crystals exhibiting spontaneous electrical polarization. They can be in two states, which can be reversed with an external electric field. When such a field is applied, the electric dipoles formed in the crystal structure of the ferroelectric material tend to align themselves with the field direction.

After the field is removed, they retain their polarization state – giving the material its non-volatile characteristic. A ferroelectric material has a non-linear relationship between the applied electric field and the polarization charge, giving the ferroelectric

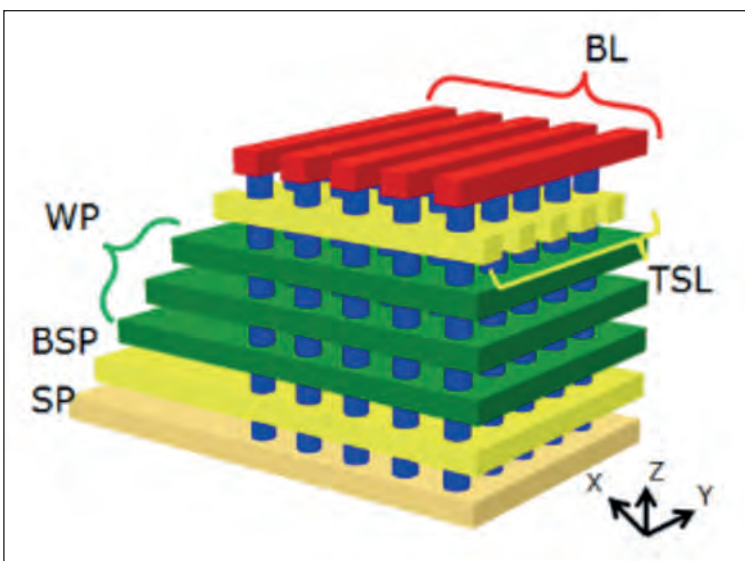
polarization-voltage (P-V) characteristic the form of a hysteresis loop.

Ferroelectric materials are being explored for DRAM-like memory applications – with ferroelectrics implemented as the dielectric in the DRAM capacitor. But one can also think of replacing the gate dielectric of a standard high-k/metal-gate transistor with a ferroelectric and end up with a non-volatile transistor: the ferroelectric FET or FeFET. The two stable, remnant polarization states of the (now ferroelectric) gate insulator modify the transistor threshold voltage, even when the supply voltage is removed.

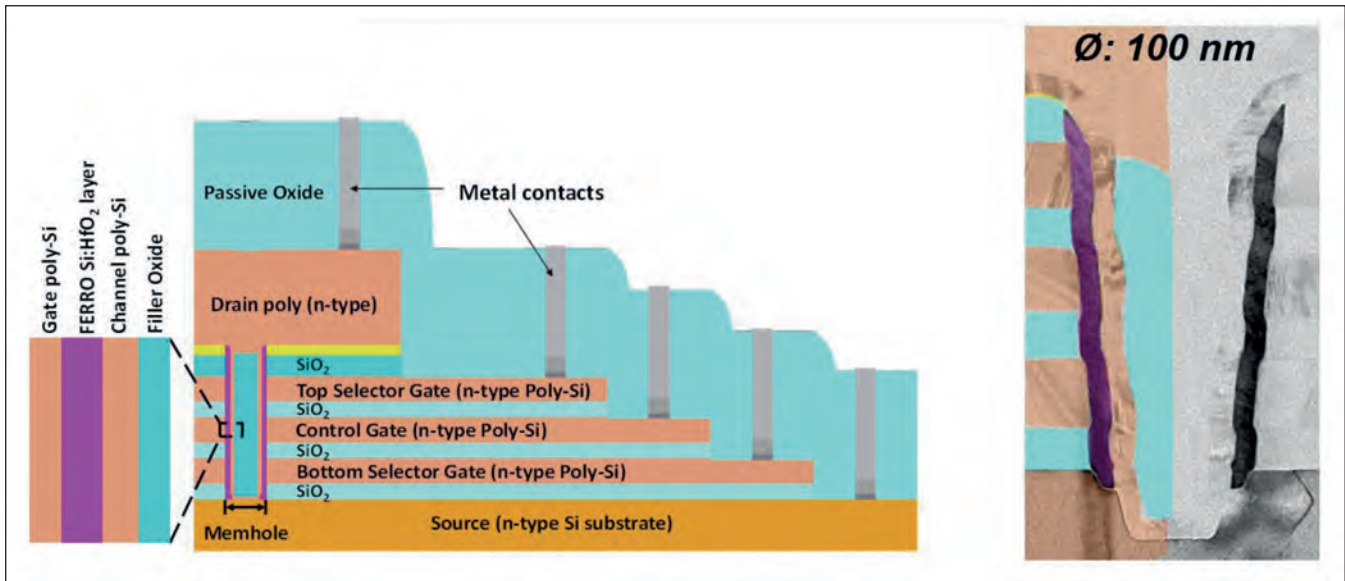
Accordingly, the binary states are encoded in the threshold voltage of the transistor. Writing of the memory cell can be done by applying a pulse on the transistor's gate which alters the polarization state of the ferroelectric material and impacts the threshold voltage. For example, applying a positive pulse lowers the threshold voltage and leaves the cell in an 'ON'-state. Reading is done by measuring the drain current. This type of memory operation resembles the working of a NAND Flash memory cell – where electrons are forced in and out of a floating gate, impacting the threshold voltage of the floating gate transistor in a similar way.

From dream to reality...

Discovered more than five decades ago, ferroelectric memory has always been considered ideal, due to its very low power needs, non-volatile character and high switching speed. However, issues with complex ferroelectric materials have presented significant challenges. Early attempts were based on ferroelectric



Schematic representation of a 3D-NAND Flash structure.



materials belonging to the perovskite family of lead-zirconate-titanate (PZT). But conformally depositing these materials in thin layers has proven very challenging. Also, the very high dielectric constant of these materials (in the order of 300) posed an obstacle for integrating them into a functional transistor. The recent discovery of a ferroelectric phase in hafnium-oxide (HfO_2), a well-known and less complex material, has however triggered a renewed interest in this memory concept.

Researchers discovered an orthorhombic crystal phase – the ferroelectric phase – that can be stabilized by doping HfO_2 with e.g. silicon (Si). Compared to PZT, HfO_2 has a lower dielectric constant and can be deposited in thin layers, in a conformal way. On top of that, HfO_2 is a well-understood material that has been used as the gate stack dielectric material in logic devices. By cleverly modifying this CMOS-compatible material, the logic transistor can now be turned into a non-volatile FeFET memory transistor.

... and from planar to vertical

Functional FeFETs have already been demonstrated in two-dimensional, planar architectures. But the ability to make conformal layers of HfO_2 opens the door towards vertical varieties, e.g. by depositing the ferroelectric material on a vertical ‘wall’ and stacking the transistors in the third dimension.

On the material side, these 3D FeFETs can solve some of the challenges imposed by 2D FeFET structures. One challenge has to do with the poly-crystalline nature of the HfO_2 dielectric. Scaling the dimensions of the HfO_2 layer significantly limits the number of crystal grains within the layer. Not all these grains have the same polarization direction, and this impacts their response on the external electric field – leading to large variabilities. By going 3D, this restriction is at least removed in the third dimension, relaxing the variability and allowing a better control of the statistics.

Vertical FeFET technology fits in a 3D-NAND-like manufacturing flow, an approach which has been actively pursued by imec. 3D-NAND Flash is today’s mainstream medium for high-density data storage. 3D NAND is relatively cheap and non-volatile, but it has a complex structure and slow memory operation.

These vertical FeFETs are expected to present several advantages over complex 3D-NAND Flash memories, including more simplified processing, lower power consumption and higher speed. Compared to 3D-NAND Flash, vertical FeFETs can potentially be programmed at much lower voltages (at about 4V compared to 20V for NAND), which leads to improved reliability and scalability.

First results: 2V memory window and Flash-like endurance

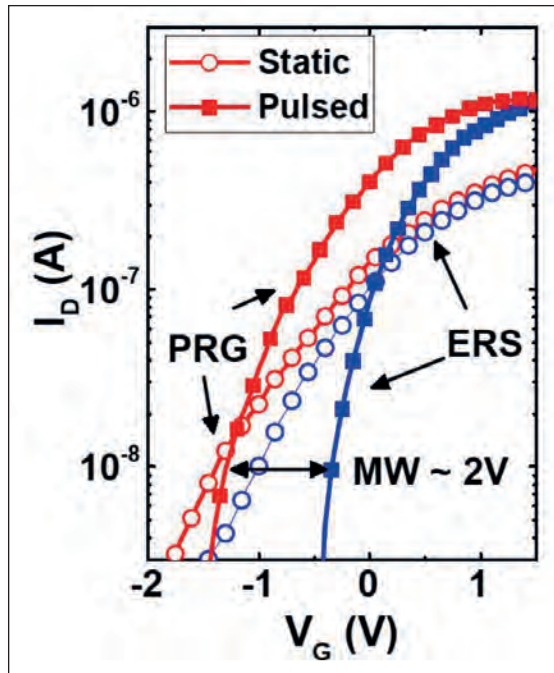
Since several years, imec has been focusing on 3D-NAND-like vertical FeFETs, hereby using its longstanding experience in advanced 3D-NAND Flash technology development combined with the tools, background and vehicles developed for earlier research on PZT-based ferroelectric memories. Since 2016, imec and its partners have an industrial affiliation program running on vertical FeFETs.

In the frame of this program, the team tackles main challenges related to the processing, characterization and reliability of the 3D FeFET. For example, the imec team is building up the knowledge on how to stabilize the orthorhombic phase of HfO_2 , which is the ferroelectric phase. This phase can be obtained by substitutional doping of the HfO_2 layer with silicon for example.

This generates a strain in the thin layer, bringing the crystal into the desired orthorhombic phase. Silicon is preferred as a dopant atom because of the thermal budget (i.e., to preserve the ferroelectric phase), but the team also studies alternative dopants such as

(Left) Schematic cross-section of the macaroni-type 3D FeFET with three cells in series; (right) TEM cross section (\varnothing : 100nm).

Memory characterization: up to 2V memory window was obtained after applying 100ns program (PRG)/erase (ERS) pulses.



aluminum (Al) and lanthanum (La), and investigates the use of hafnium-zirconium-oxide as an alternative ferroelectric.

Recently, imec demonstrated a first functional vertical ferroelectric HfO_2 FET based on a 3D macaroni NAND architecture. The device was fabricated based on imec's process flow for 3D-NAND Flash memories, now replacing the typical oxide-nitride-oxide (ONO) dielectric layer by an 8nm Si-doped HfO_2 layer – which is deposited using atomic layer deposition (ALD).

Poly-Si is used as the gate material, and amorphous Si for the channel. The test vehicle contains a vertical string of three gates in series (a control gate, and a bottom and top selector gate). The hole in the string is filled with oxide and then recessed, giving it a macaroni-like structure. In a real 3D-NAND-like device, the number of control gates can mount up to 64 in the vertical direction to obtain a high-density memory solution.

For this test vehicle, up to 2V memory window was obtained after applying 100ns program/erase pulses. The FeFET exhibits 85°C retention: after 100 hours at 85°C, a clear separation of states can still be observed. The team also reported Flash-like endurance of 104 cycles and has performed first reliability assessments. Charge trapping – caused by high fields over the interface – is put forward as the limiting factor for the cycling performance. A decrease of the interface layer thickness could potentially address this challenge.

3D-NAND-like applications and machine learning

FeFETs are still in the early stages of R&D and it's

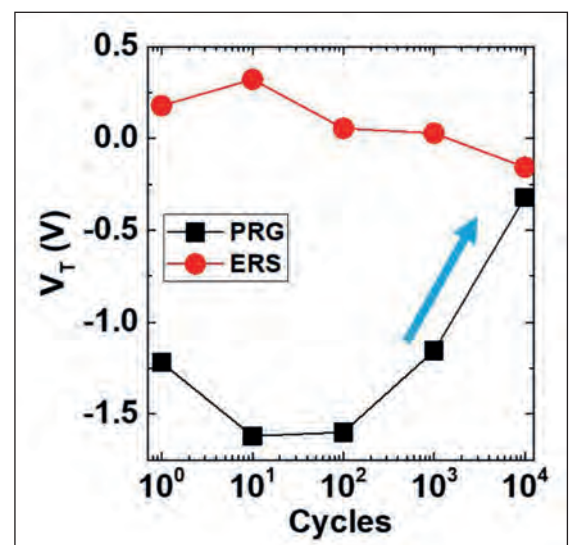
too soon to say if or when they will ever make it into production. Nevertheless, this promising new memory concept has raised major interest from the industrial players. It is the role of imec to explore its full potential and offer its partners a head start in this exciting research area. They can then decide how to best fit FeFET memories in their products and chips.

As a standalone memory, FeFETs are believed to enter the family of storage class memories (SCMs) and as such help closing the gap between fast, volatile DRAM and slow, non-volatile and high-density NAND Flash memories. FeFETs are non-volatile and can offer several advantages over NAND Flash: they have faster switching speeds, are simpler to process, consume less power and can potentially operate at much lower voltages. But, although closer to DRAM in terms of speed, the limited cycling performance (104 for FeFET compared to 1012 for DRAM) will most probably push FeFETs to the NAND side of the DRAM-NAND gap.

FeFET memories have also gained interest among the logic foundries: the memory's high speed can be very advantageous for machine learning applications, which rely on in-memory computing. For this, several types of memories, including Flash, magnetic random access memory (MRAM), resistive RAM, phase change memory (PCM), static RAM (SRAM) and FeFET, are currently being explored. The non-linear characteristics and speed properties of FeFETs make the technology particularly appealing for machine learning applications that make use of deep learning convolutional neural network models. For this application, we will most probably see planar versions of FeFETs coming up.

Outlook: towards higher density FeFETs

A particular advantage of NAND-Flash technology is



Reliability characterization: Evolution of the threshold voltage V_T with cycling after program and erase. Closing of the memory window is observed after 104 cycles.

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As a standalone memory, FeFETs are believed to enter the family of storage class memories (SCMs) and as such help closing the gap between fast, volatile DRAM and slow, non-volatile and high-density NAND Flash memories

the ability to store up to 4 bits per cell, which gives the technology its unique high data density. In a traditional single-level cell, each cell can be in one of two binary states, storing one bit of information per cell. Industrial NAND-Flash cells have evolved from single-level cells to cells with 2, 3 and even 4 bits per cell. With 4 bits, the cells use 16 discrete charge levels in each individual transistor – requiring a sufficiently large memory window.

For FeFETs, imec sees three ways to increase the data density and make FeFETs true competitors for NAND Flash in terms of density. First, provided that the threshold voltage can be sufficiently stabilized, the 2 – 2.5V memory window of FeFETs should in principle allow programming 2 bits per cell – which requires 4 charge levels within the transistor.

Second, the cell density can be doubled by using a trench-like architecture for connecting the transistors, with two transistors on each side of the trench. In current 3D FeFET designs, such as in imec's macaroni NAND architecture, the control gate is designed in a gate-all-around (GAA) structure. This means that the gate is wrapped around the channel, limiting the number of transistors (per layer and per string) to one.

The GAA structure is needed in NAND Flash memories to improve the injection of charges into the floating gate or the nitride trapping layer but is not needed for FeFETs. Imec is currently exploring the use of an alternative trench-like structure, where the transistors are implemented at the sidewall of a trench – with two transistors now at opposite ends of the trench. This type of structure should potentially allow doubling the cell density while decreasing the variability between cells.

And third, the FeFET memory cell can potentially be scaled to much smaller physical dimensions. In a typical NAND Flash cell, the ONO dielectric layer has a thickness of about 20nm. In a FeFET cell, the HfO₂ ferroelectric layer is expected to scale down to 4nm. In addition, in the vertical direction, the lower operation voltage of the FeFET compared to NAND Flash will

allow the word lines to come closer together.

In summary, these possible routes towards higher density in combination with a higher speed, non-volatile, Flash-like endurance, lower operation voltage and lower power consumption make 3D FeFETs interesting contenders for 3D NAND-like applications.

Want to know more?

The paper 'Vertical ferroelectric HfO₂ FET based on 3D NAND architecture: towards dense low-power memory' by K. Florent et al. was presented at the 2018 IEDM conference, and can be requested via our contact form.

If you want more information on ferroelectric memories, you can request the following papers via our contact form: (1) 'Memory technology for the terabit era: from 2D to 3D', Symp. on VLSI Technology, Kyoto, Japan, June 2017, invited, p. T24-25; (2) '3D memories and ferroelectrics', 2017 IEEE-IMW, Monterey, CA, invited, p. 92-94.



About Jan Van Houdt

Jan Van Houdt received a Ph.D. from the KU Leuven. During his PhD work, he invented the HIMOS™ Flash memory, which he transferred to several industrial production lines. In 1999, he became responsible for Flash memory at imec and as such was the driving force behind the expansion of imec's Industrial Affiliation Program on Memory Technology. Jan has published more than 300 papers in international journals and accumulated more than 250 conference contributions (incl. ~50 invitations and 5 best paper awards). He has filed about 80 patents and served on the program and organizing committees of 10 major semiconductor conferences. In 2014, he received the title of IEEE Fellow for his contributions to Flash memory devices. In the same year, he started the Ferroelectrics program at imec and became a guest professor at the KU Leuven teaching on CMOS and memory technology. Today, he is Scientific Director at imec, active both in the memory as well as in the logic scaling programs.

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US Patent numbers:
10,597,773 10,711,343

1

High
beam
current

2

Longer
source
life

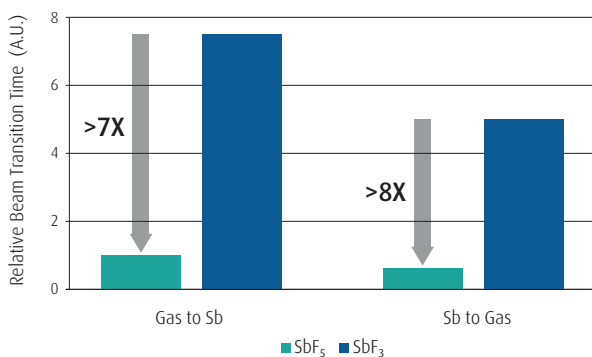
3

Fast
beam
switching

4

Easy
handling
& transport

Relative transition times comparison
SbF₅ vs SbF₃



Antimony to Boron beam transition
SbF₅ vs Sb₂O₃

